TB-FMCL-MIPI-DIRECT Hardware User Manual

Rev.1.00

Revision History

Version	Date	Description	Publisher
Rev.0.99	5/17/2019	Initial draft	ST
Rev.1.00	5/23/2019	Released.	ST

Table of Contents

List of Figures

List of Tables

Introduction

Thank you for purchasing the **TB-FMCL-MIPI-DIRECT** board. Before using the product, be sure to carefully read this user manual and fully understand how to correctly use the product. First read through this manual, and then always keep it handy.

SAFETY PRECAUTIONS

Be sure to observe these precautions!

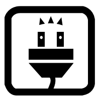
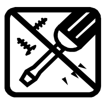
Observe the precautions listed below to prevent injuries to you or other personnel or damage to property.

- **Before using the product, read these safety precautions carefully to assure correct use.**
- **These precautions contain serious safety instructions that must be observed.**
- **After reading through this manual, be sure to always keep it handy.**

The following conventions are used to indicate the possibility of injury/damage and classify precautions if the product is handled incorrectly.

⚠ **Danger**	Indicates the high possibility of serious injury or death if the product is handled incorrectly.
⚠ **Warning**	Indicates the possibility of serious injury or death if the product is handled incorrectly.
⚠ **Caution**	Indicates the possibility of injury or physical damage in connection with houses or household goods if the product is handled incorrectly.

The following graphical symbols are used to indicate and classify precautions in this manual.
(Examples)

	Turn off the power switch.
	Do not disassemble the product.
	Do not attempt this.

Warning

	In the event of a failure, disconnect the power supply. If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately and contact our sales personnel for repair.
	If an unpleasant smell or smoking occurs, disconnect the power supply. If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately. After verifying that there is no smoking, contact our sales personnel for repair.
	Do not disassemble, repair or modify the product. Otherwise, a fire or electric shock may occur due to a short circuit or heat generation. For inspection, modification or repair, contact our sales personnel.
	Do not touch a cooling fan. As a cooling fan rotates at high speed, do not put your hand close to it. Otherwise, it may cause injury to persons. Never touch a rotating cooling fan.
	Do not place the product on unstable locations. Otherwise, it may drop or fall, resulting in injury to persons or failure.
	If the product is dropped or damaged, do not use it as is. Otherwise, a fire or electric shock may occur.
	Do not touch the product with a metallic object. Otherwise, a fire or electric shock may occur.
	Do not place the product in dusty or humid locations or where water may splash. Otherwise, a fire or electric shock may occur.
	Do not get the product wet or touch it with a wet hand. Otherwise, the product may break down or it may cause a fire, smoking or electric shock.
	Do not touch a connector on the product (gold-plated portion). Otherwise, the surface of a connector may be contaminated with sweat or skin oil, resulting in contact failure of a connector or it may cause a malfunction, fire or electric shock due to static electricity.

Caution	
⃠	**Do not use or place the product in the following locations.** • Humid and dusty locations • Airless locations such as closet or bookshelf • Locations which receive oily smoke or steam • Locations exposed to direct sunlight • Locations close to heating equipment • Closed inside of a car where the temperature becomes high • Static-prone locations • Locations close to water or chemicals Otherwise, a fire, electric shock, accident or deformation may occur due to a short circuit or heat generation.
⃠	**Do not place heavy things on the product.** Otherwise, the product may be damaged.

■ Disclaimer

This product is a MIPI interface for Xilinx FPGA evaluation boards. Tokyo Electron Device Limited assumes no responsibility for any damages resulting from the use of this product for purposes other than those stated.

Even if the product is used properly, Tokyo Electron Device Limited assumes no responsibility for any damages caused by:

(1) Earthquake, thunder, natural disaster or fire resulting from the use beyond our responsibility, acts by a third party or other accidents, the customer's willful or accidental misuse, or use under other abnormal conditions.

(2) Secondary impact arising from use of this product or its unusable state (business interruption or others)

(3) Use of this product against the instructions given in this manual.

(4) Malfunctions due to connection to other devices.

Tokyo Electron Device Limited assumes no responsibility or liability for:

(1) Erasure or corruption of data arising from use of this product.

(2) Any consequences or other abnormalities arising from use of this product, or

(3) Damage of this product not due to our responsibility or failure due to modification.

This product has been developed by assuming its use for research, testing or evaluation. It is not authorized for use in any system or application that requires high reliability.
Repair of this product is carried out by replacing it on a chargeable basis, not repairing the faulty devices. However, non-chargeable replacement is offered for initial failure if such notification is received within two weeks after delivery of the product.
The specification of this product is subject to change without prior notice.
The product is subject to discontinuation without prior notice.

1. Related Documents and Accessories

Documents related to the TB-FMCL-MIPI-DIRECT can be retrieved from http://solutions.inrevium.com/ http://solutions.inrevium.com/jp/ or by contacting your Sales person.

Table 1-1 Accessories

Description	Manufacturer	Quantity
Spacer, 10mm, M2.6	Hirosugi	2
Spacer, 25mm, M2.6	Hirosugi	2
Screw, 6mm, M2.6 w/ washers	Hirosugi	6

2. Overview

The TB-FMCL-MIPI-DIRECT is an ANSI/VITA 57.1 compatible FPGA Mezzanine Card (FMC) with a Low-Pin-Count (LPC) connector that presents two separate 4-lane MIPI ports to a pair of 40-pin sockets located in the FMC I/O Window. Each port presents five MIPI lanes (4 data plus clock) with direct, non-translated or isolated connections to FPGA SelectIO pairs provided at the FMC connector.

The TB-FMCL-MIPI-DIRECT does not utilize any of the high-speed serial DPx data links and GBTCLKs provided in the FMC standard, so present data speed is limited to the capabilities of HR and/or HP SelectIO of Xilinx FPGAs. HP IO can support higher rates, providing more options for higher framerate video formats (such as 3D). The PCB design can readily support at least 2.5 Gb/s per lane, providing accommodation for future advanced FPGA platforms featuring super speed SelectIO.

Table 2-1 Example Video Frame rates for 4-lane MIPI

Video Resolution	Frame Rate at 10-Bits per Pixel 4:2:2 format	MIPI data Rate
7680x4320 (8K UHD)	30fps	4 lanes @ 2.5Gbps per lane
3840x2160 (UHD)	60 fps	4 lanes @ 1.2Gbps per lane
1920x1080 (HD)	120 fps	4 lanes @ 800Mbps per lane

The TB-FMCL-MIPI-DIRECT is produced as a dual MIPI card that supports two 4-lane bi-directional MIPI ports on a single FMC LPC module. The lane directions are entirely determined by the circuitry implemented in the FPGA. To communicate with MIPI peripherals, the FPGA IOs must comply with MIPI Alliance Specification for D-PHY (vers. 1.00.00, May 2009) electrical and timing parameters of the LP and HS protocols described in the specification.

3. Features

FMC LPC Main Connector	Samtec ASP-134604-01
MIPI Connectors	Samtec LSHM-120-01-F-DH-A-N-K-TR
Four MIPI GPIO ports	direction individually selectable
MIPI I2C port	Dedicated I2C port per MIPI connector
MIPI GPIO and I2C Voltage	Individually jumper selected: VADJ, VUSER, 2.5V, 3.3V
Selectable MIPI VUSER up to 0.8A	Teas Instruments TPS62150 Buck converter for 1.5/1.8/2.5/3.3V. One VUSER services both ports.
FPGA VADJ GPIO Signal Level	1.2V through 3.3V using voltage level translators. 1.2V is recommended due to Xilinx VCCO requirement for MIPI DPHY IO
12V power up to 200mA per MIPI	PTC self-resetting fuse protected Cooper PTS120615V050
LDO regulators for PHYs	Texas Instruments TPS74701 generating local 2.5V
FMC Configuration EEPROM	Micron M24C02 2Kb I2C EEPROM with GA0/1 address selection
Voltage presence LED indicators	One green LED for each on-board voltage rail

An excerpt from ANSI/VITA 57.1 of the FMC LPC connector physical pin layout is provided below. The TB-FMCL-MIPI-DIRECT implements only the LPC sub-portion as defined for rows C, D, G, and H. All other rows apply to the FMC HPC implementation and are left open-circuit when the TB-FMCL-MIPI-DIRECT is installed in an FMC HPC receptacle. Pin signal names shown are per VITA 57.1 definition.

	K	J	H	G	F	E	D	C	B	A
1	NC	NC	VREF_A_M2C	GND	NC	NC	PG_C2M	GND	NC	NC
2	NC	NC	PRSNT_M2C_L	CLK1_M2C_P	NC	NC	GND	DP0_C2M_P	NC	NC
3	NC	NC	GND	CLK1_M2C_N	NC	NC	GND	DP0_C2M_N	NC	NC
4	NC	NC	CLK0_M2C_P	GND	NC	NC	GBTCLK0_M2C_P	GND	NC	NC
5	NC	NC	CLK0_M2C_N	GND	NC	NC	GBTCLK0_M2C_N	GND	NC	NC
6	NC	NC	GND	LA00_P_CC	NC	NC	GND	DP0_M2C_P	NC	NC
7	NC	NC	LA02_P	LA00_N_CC	NC	NC	GND	DP0_M2C_N	NC	NC
8	NC	NC	LA02_N	GND	NC	NC	LA01_P_CC	GND	NC	NC
9	NC	NC	GND	LA03_P	NC	NC	LA01_N_CC	GND	NC	NC
10	NC	NC	LA04_P	LA03_N	NC	NC	GND	LA06_P	NC	NC
11	NC	NC	LA04_N	GND	NC	NC	LA05_P	LA06_N	NC	NC
12	NC	NC	GND	LA08_P	NC	NC	LA05_N	GND	NC	NC
13	NC	NC	LA07_P	LA08_N	NC	NC	GND	GND	NC	NC
14	NC	NC	LA07_N	GND	NC	NC	LA09_P	LA10_P	NC	NC
15	NC	NC	GND	LA12_P	NC	NC	LA09_N	LA10_N	NC	NC
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	NC	NC
17	NC	NC	LA11_N	GND	NC	NC	LA13_P	GND	NC	NC
18	NC	NC	GND	LA16_P	NC	NC	LA13_N	LA14_P	NC	NC
19	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	NC	NC
20	NC	NC	LA15_N	GND	NC	NC	LA17_P_CC	GND	NC	NC
21	NC	NC	GND	LA20_P	NC	NC	LA17_N_CC	GND	NC	NC
22	NC	NC	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	NC	NC
23	NC	NC	LA19_N	GND	NC	NC	LA23_P	LA18_N_CC	NC	NC
24	NC	NC	GND	LA22_P	NC	NC	LA23_N	GND	NC	NC
25	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	NC	NC
26	NC	NC	LA21_N	GND	NC	NC	LA26_P	LA27_P	NC	NC
27	NC	NC	GND	LA25_P	NC	NC	LA26_N	LA27_N	NC	NC
28	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	NC	NC
29	NC	NC	LA24_N	GND	NC	NC	TCK	GND	NC	NC
30	NC	NC	GND	LA29_P	NC	NC	TDI	SCL	NC	NC
31	NC	NC	LA28_P	LA29_N	NC	NC	TDO	SDA	NC	NC
32	NC	NC	LA28_N	GND	NC	NC	3P3VAUX	GND	NC	NC
33	NC	NC	GND	LA31_P	NC	NC	TMS	GND	NC	NC
34	NC	NC	LA30_P	LA31_N	NC	NC	TRST_L	GA0	NC	NC
35	NC	NC	LA30_N	GND	NC	NC	GA1	12P0V	NC	NC
36	NC	NC	GND	LA33_P	NC	NC	3P3V	GND	NC	NC
37	NC	NC	LA32_P	LA33_N	NC	NC	GND	12P0V	NC	NC
38	NC	NC	LA32_N	GND	NC	NC	3P3V	GND	NC	NC
39	NC	NC	GND	VADJ	NC	NC	GND	3P3V	NC	NC
40	NC	NC	VADJ	GND	NC	NC	3P3V	GND	NC	NC
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

Figure 3-1 FMC LPC Connector Pinout per VITA 57.1

4. Block Diagram

Figure 4-1 shows the TB-FMCL-MIPI-DIRECT block diagram.

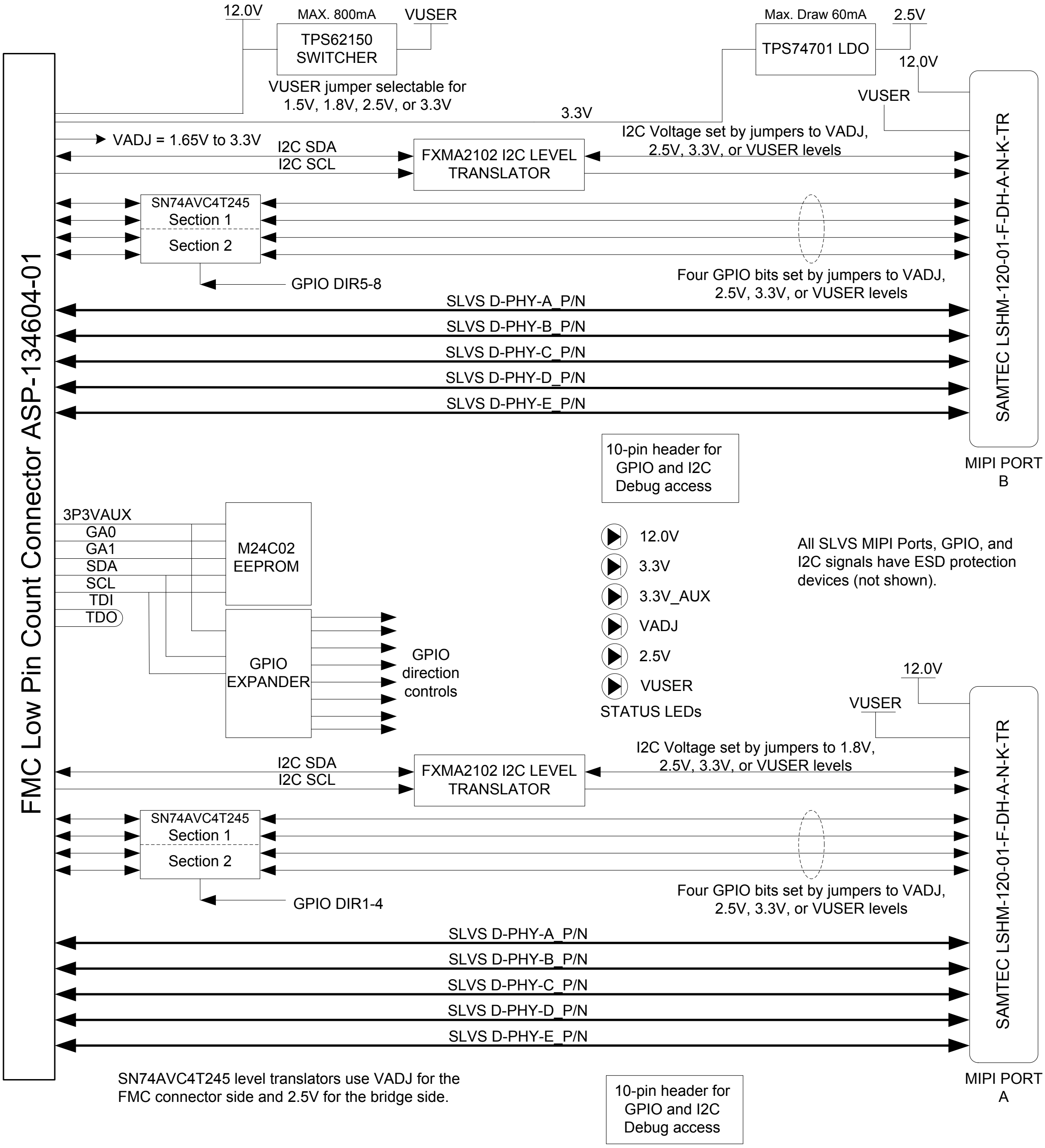


Figure 4-1 TB-FMCL-MIPI-DIRECT Block Diagram

5. External View of the Board

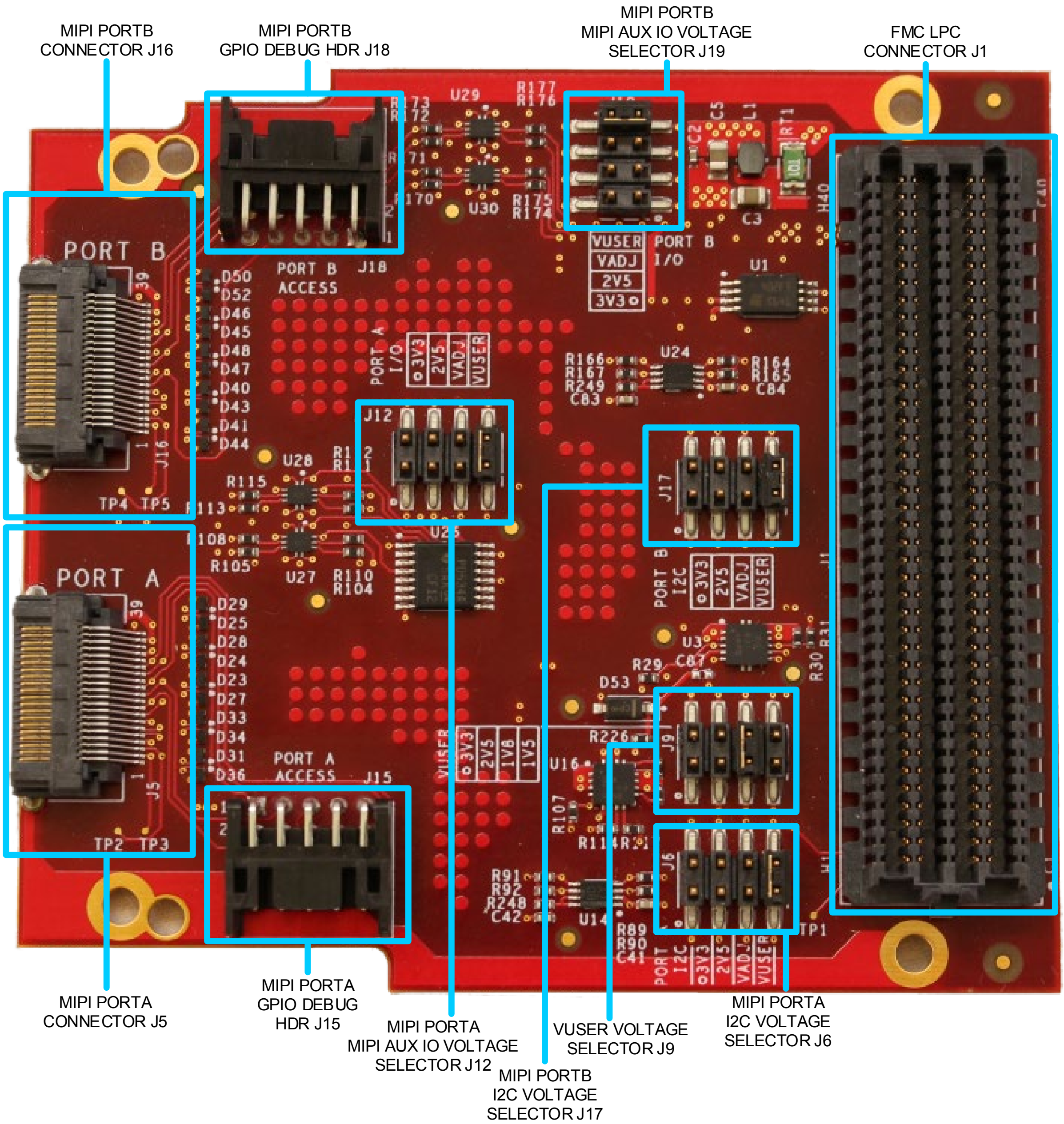


Figure 5-1 Photo of TB-FMCL-MIPI-DIRECT (Side 1)

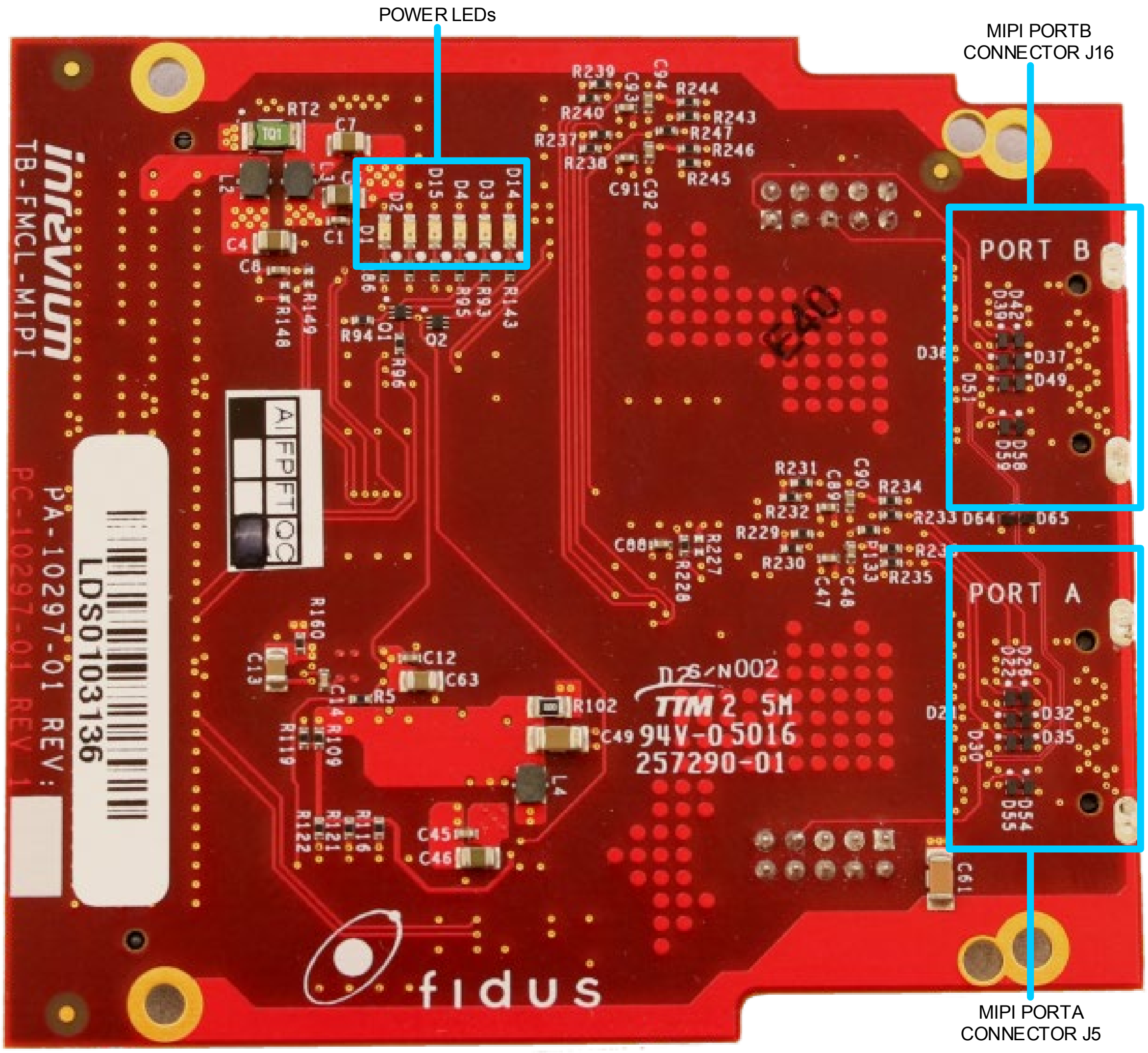


Figure 5-2 Photo of TB-FMCL-MIPI-DIRECT (Side 2)

6. Board Specification

The following shows the TB-FMCL-MIPI-DIRECT board physical specifications.

External Dimensions	76.50 mm L x 69.00 mm W – Dimensions/features per VITA57.1
Number of Layers	8 layers
Board Thickness	1.6 mm
Material	FR370HR
FMC LPC Connector	Samtec ASP-134604-01
MIPI Connectors	Samtec LSHM-120-01-F-DH-A-N-K-TR

Note: Refer to samtec.com for MIPI mating connector

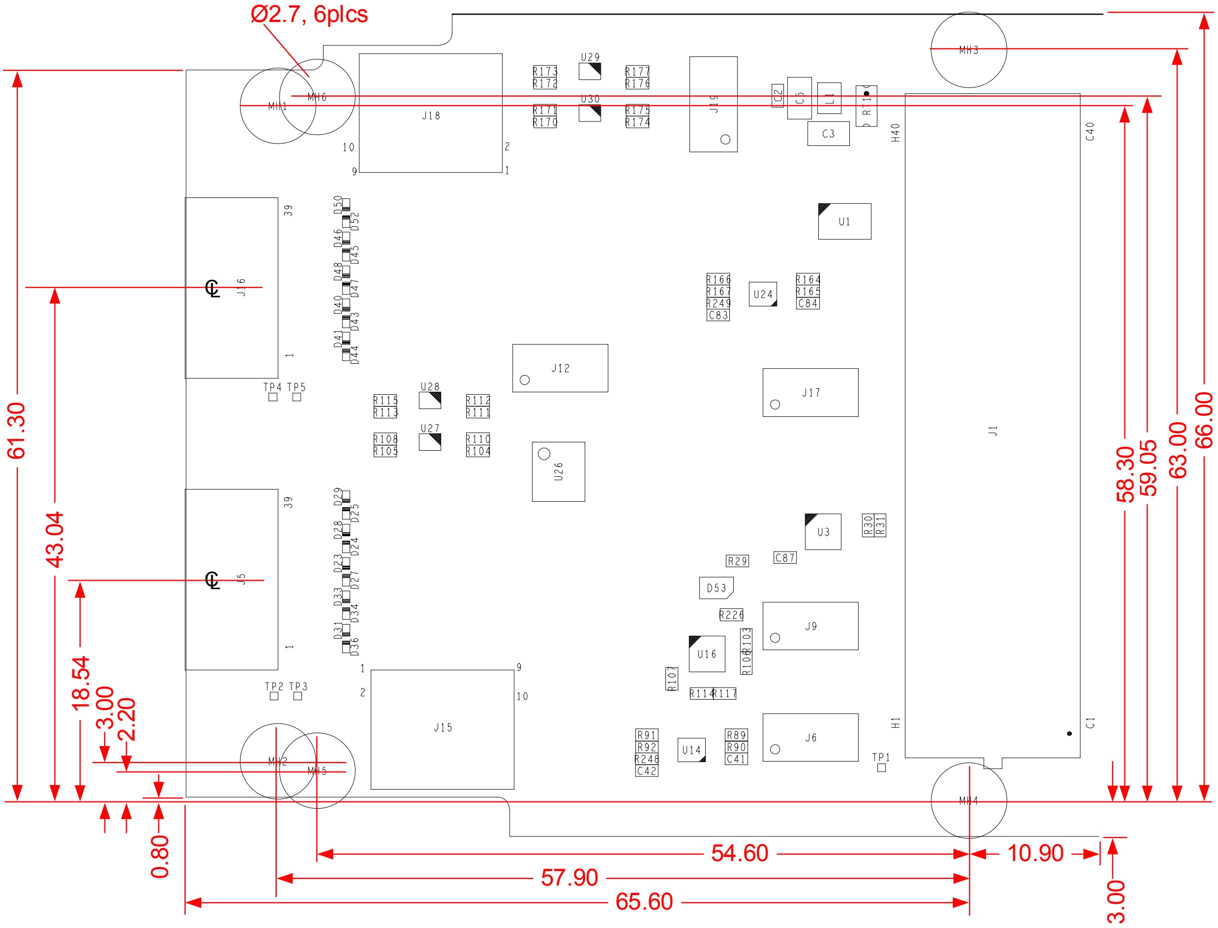


Figure 6-1 TB-FMCL-MIPI-DIRECT Board Dimensions (mm)

Notes:

- Board outline features conform to VITA57.1 air-cooled commercial grade single-width modules
- MIPI connectors are pitched at 24.50mm center-to-center.
- MIPI position 1 is defined as MIPI Port A (J5), MIPI position 2 is defined as MIPI Port B (J16)
- Board component side is defined in VITA 57.1 as Side 1 and faces the host carrier card when installed
- Board solder side is defined as Side 2 and is probing and visually accessible when the card is installed

7. Board Power System

7.1. Power System Overview

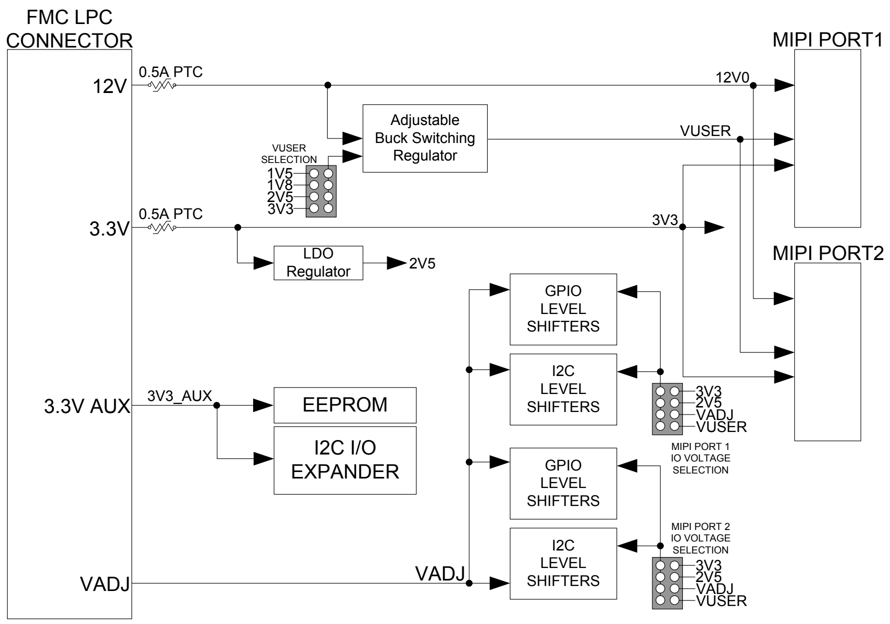


Figure 7-1 shows the TB-FMCL-MIPI-DIRECT power supply structure. The card uses the 12 Volt, the 3.3 Volt, the 3.3V AUX, and the VADJ rails supplied on the FMC connector from the carrier card. There is one 2.5V LDO regulator for a fixed IO voltage selection, and one switching regulator to generate the MIPI VUSER voltage rail. VADJ can range from 1.2V to 3.3V and is used mainly for the GPIO and I2C voltage translators. There is no control of power sequencing. The 12V and 3.3V rails are protected by 0.5Amp PTC resettable fuses. If either fuse trips due to an overcurrent fault, remove power to the card and wait a minute for the fuse to cool. Remove the condition causing the excess current and apply power. If the fuse trips again, remove power, wait for the fuse to cool, remove the card from the carrier, and contact our sales personnel for repair.

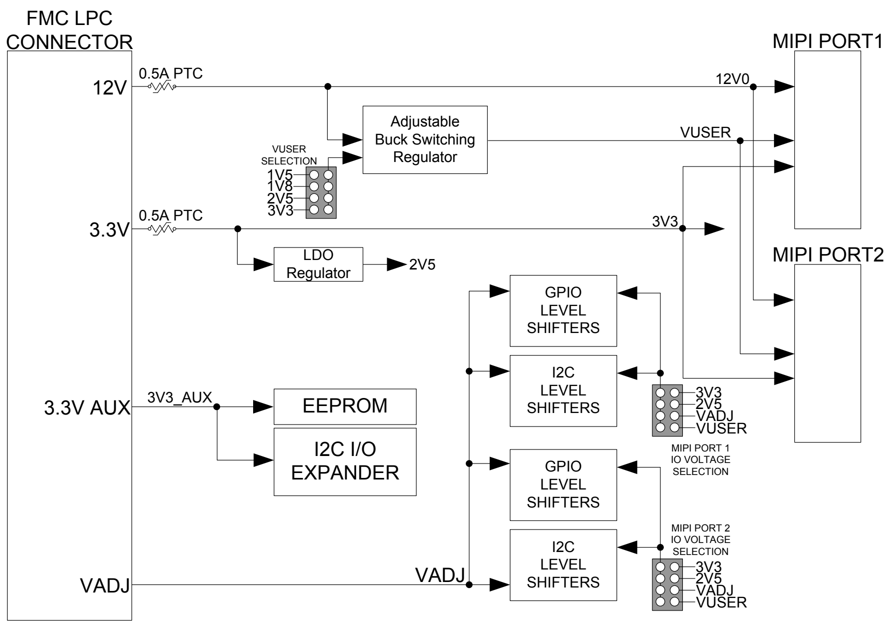


Figure 7-1 TB-FMCL-MIPI-DIRECT Power Structure

7.2. MIPI User Power Rail

The MIPI User power source connector power is supplied from a Texas Instruments TPS62150 switching regulator. It provides four user selectable output voltages from 1.5V to 3.3V at a total current of 800mA, or 400mA per MIPI port. The VUSER voltage does not necessarily need to reflect the MIPI IO logic levels, however, it is available as one of the level shifter reference options. The VUSER selection jumper is mapped as follows:

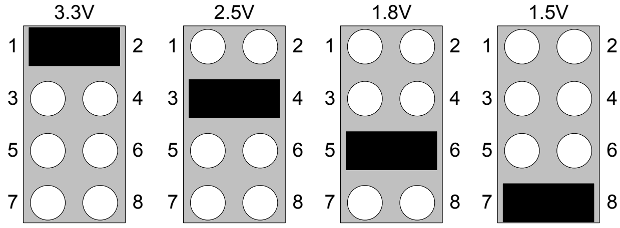


Figure 7-2 VUSER Jumper Select Positions

Note: Installing more than one shunt, or positioning the shunt in a position other than shown may result in permanent damage to the board.

7.3. LDO regulator

The Texas Instruments TPS74701 LDO is set for 2.5V output and can be used to power level shifters and pull-ups (4.5mA maximum loading from MIPI I2C pullups if 2.5V is selected as the IO voltage option for all the MIPI GPIO and I2C ports). Note that the TPS74701 requires a bias voltage of 1.3V greater than the **output** voltage, thus the 2.5V regulator requires a bias input of at least 3.8V. Since there is no 5V rail available, the bias input is generated by a Zener diode from the FMC 12V power. The Zener regulation system draws 4.6mA (typ.) to account for Bias current variation while still providing sufficient reverse Zener current to establish a stable voltage of approximately 4.3V.

The regulator provides a Power-Good output; this open-collector output drives LED indicator D4 when the output voltage has stabilized at 2.5V.

7.4. LED Power Indicators

A series of six green LEDs are located in a row on Side 2 (solder side) so they are visible when the card is installed on an FMC carrier. The LEDs indicate the presence of the various supply rails, and under normal conditions, all six LEDs should be lit when the card is powered-up. The following diagram of the solder side displays the row of LEDs and their meaning:

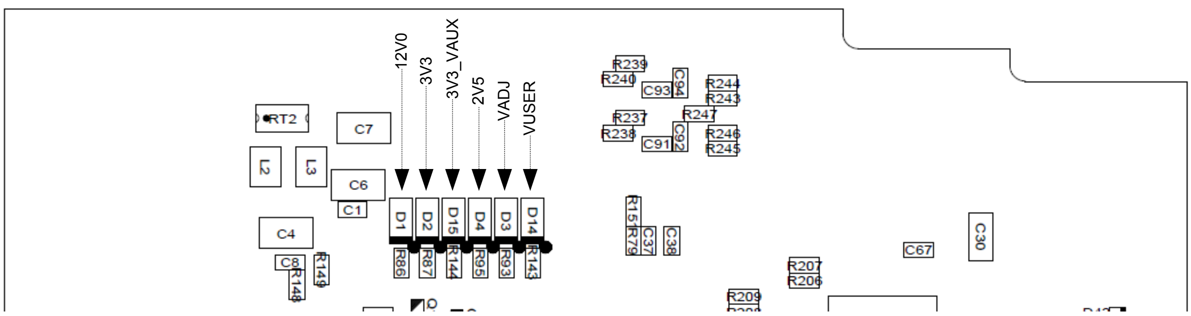


Figure 7-3 Power LEDs Identification

8. MIPI IO Signals

8.1. MIPI Signaling brief

The MIPI Alliance D-PHY Specification describes the electrical and operational protocol of the MIPI lanes. In summary, the lanes conduct point-to-point data transactions using a combination of 1.2V LVCMOS state signaling termed LP (Low Power), and 400mV SLVS (Scalable Low Voltage Signaling) termed HS (High Speed), combined on a single physical pair for each lane. The HS mode is the primary payload data phase and can operate up to 2.5 Gb/s, conforming electrically to the JEDEC® 8-13 SLVS specification. The LP mode, used primarily for protocol handshake, can also transfer facility data at up to 20 Mb/s. A single clock lane accompanies the data lanes of each MIPI port, operating under the same LP handshake protocol and using the same SLVS mode when active. The clock signal maintains a DDR (Double Data Rate) quadrature relationship with the HS data bursts, placing a rising or falling edge nominally in the center of each data bit time across all associated data lanes.

It is important to understand that MIPI is not meant for externally accessible IO ports. For that reason, strong line drivers, receiver AGC/equalization, and ESD robustness measures are not typically present in MIPI line interfaces, strictly limiting peripheral interconnect lengths to well under 35cm when operating at the 1 Gb/s nominal top speed suggested in the D-PHY Specification.

8.2. MIPI D-PHY Lanes

Each MIPI connector provides five differential pairs designed to interface to 100-ohm differential SLVS wiring to the MIPI peripheral. The differential pairs are assigned per Samtec's recommendations for the LSHM series where each pair occupies adjacent pins bounded on both sides by GND pins. For signal integrity reasons, in the 20-pin by 2-row connector pin matrix, the high-speed differential lanes occupy the inside row, or "short" path (ROW 1), of the connector. The HS burst timing demands tight delay matching between all lanes, thus all five lanes of each port from MIPI connector to FMC connector pins are delay matched to better than 10ps, supporting speeds up to 2.5 Gb/s.

CAUTION: A direct DC path is required from FMC to MIPI connector to support the D-PHY protocol, thus only MIPI D-PHY compliant peripherals should be connected to the MIPI ports. Connecting any other type of device may result in damage to the IOs of the FMC host platform FPGA. Ensure that maximum transient voltage limits of the host FPGA IOs are not exceeded in receive applications. In addition, the MIPI D-PHY Specification stipulates maximum transient voltage limits of +1.45V / -0.150V on SLVS lanes. Ensure that FPGA IOs driving SLVS lanes (transmit application) are appropriately configured for the 1.2V D-PHY standard, and that the transient limits are not exceeded by default IO states prior to and/or during FPGA configuration.

The D-PHY Specification stipulates a maximum lane flight time (propagation delay) of 2.0 nanoseconds, which corresponds to a maximum trace length of between 250 to 300mm for typical PCB and flex substrates. Available distance can be computed by the formulas:

Max. Lane length (cm) = 54cm / $\sqrt{\varepsilon}$ (dielectric constant)

Lane Delay (nsec) = 2*(trace length / Max. lane length)

The host platform layout design must be examined when using the TB-FMCL-MIPI-DIRECT card due to the maximum flight time limit, particularly since MIPI is a short-run point-to-point media interface. In addition to minimizing lane delay skew, care must be taken to ensure the MIPI lane traversal distance on the FPGA host board is short enough to leave practical length headroom at the MIPI connector after accounting for the FMC card trace and connector delays. Also be aware that different FMC positions will likely have different trace lengths on a multiple FMC port carrier card. Neglecting the propagation delay limit may result in unreliable HS data transfers at best, and complete inability to transfer HS data at worst.

All MIPI trace length from FMC footprint to Port A connector footprint ~ 84.6mm
All MIPI trace length from FMC footprint to Port B connector footprint ~ 83.8mm

8.3. MIPI GPIO Signals

Each MIPI connector is supplied with four GPIO signals that are supplied through level translators from FPGA SelectIO pins on the FMC connector, as per the following diagram:

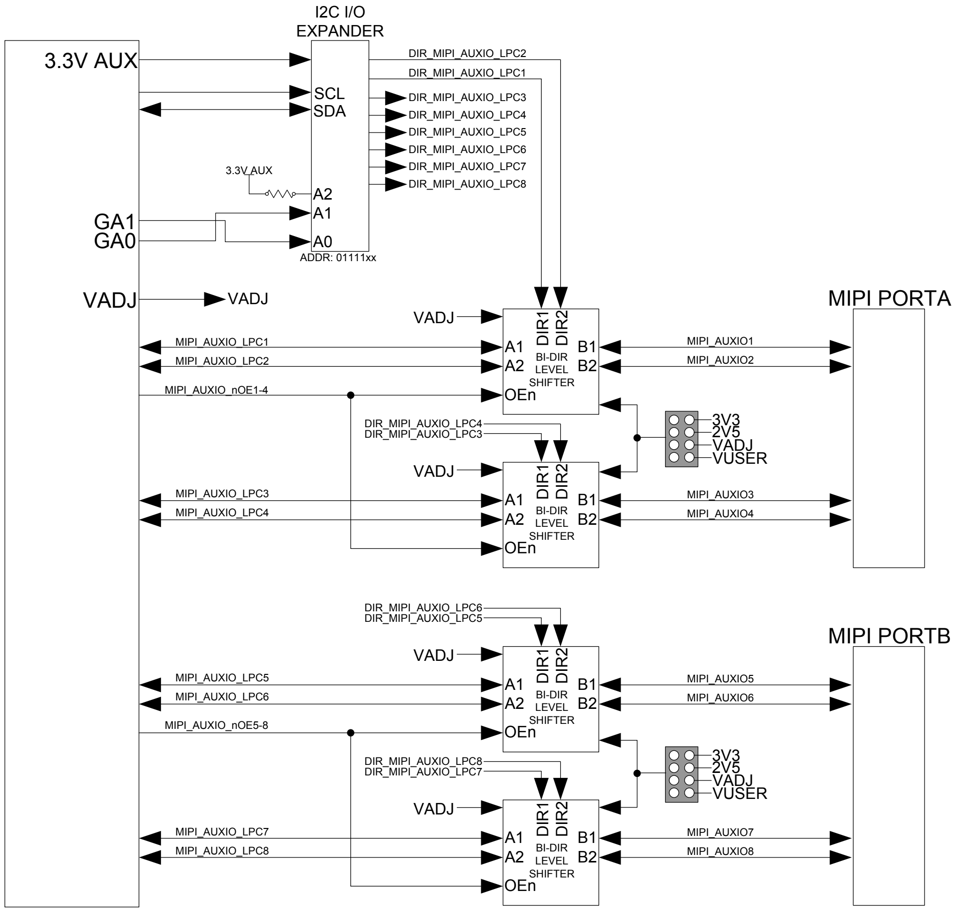


Figure 8-1 GPIO SIGNALS TO EACH MIPI PORT

The VADJ IO voltage domain of the FMC is level shifted to the user selected MIPI IO voltage domain using Texas Instruments SN74AVC2T245 bi-directional dual-voltage transceivers. These devices can operate to voltages as low as 1.2V (this corresponds to the VCCO specified by Xilinx for MIPI DPHY IO type) . Two FPGA pins on the FMC connector control the output enable (OEn) of the level shifters (OEn=1 results in Hi-Z on each side of translator). Each MIPI connector GPIO group can have its MIPI IO voltage selected from four options as shown:

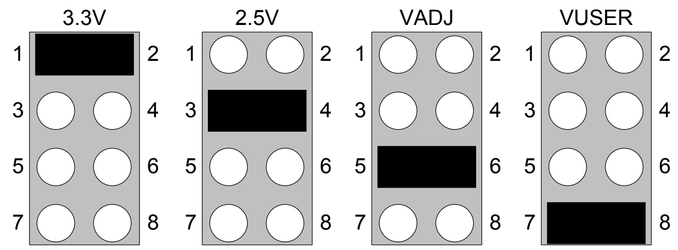


Figure 8-2 MIPI GPIO Voltage Select Options

Each GPIO group has a header for voltage selection; MIPI PORT A MIPI_AUXIO_(1-4) uses header J12, and MIPI PORT B MIPI_AUXIO_(5-8) uses header J19.

The direction of each of the eight GPIOs is determined by the Carrier Card FPGA via the MIPI FMC's I2C I/O Expander (Texas Instruments, PCA9534A). The I/O Expander is powered by 3V3_AUX and is located on the dedicated FMC I2C bus at address: 01111xx (xx is determined by the FMC slot signals GA[0:1]; GA0 → A1, GA1 → A0). The I/O Expander's GPIOs default to input upon power up. Once configured, when direction control pin is "high", the GPIOs are outputs driven to the MIPI Port connector. When the direction control pin is "low", the GPIOs are inputs driven from the MIPI Port connector.

To help avoid contention, the recommended configuration sequence for the I/O Expander and Buffers are as follows:

Table 8-1 GPIO Signals: Recommended sequencing

Stage	Action	Signals
T0	Power-Up, FPGA Configuration	MIPI_AUXIO_nOE1-4 = 1 MIPI_AUXIO_nOE5-8 = 1 DIR_MIPI_AUXIO_LPC[1:8]= X (don't Care) MIPI_AUXIO_LPC[1:8] = X (don't care) Notes: 1. Both OE signals have resistor pull-ups to VADJ 2. Direction control signals have resistor pull-downs
T1	Program I/O Expander	MIPI_AUXIO_nOE1-4 = 1 MIPI_AUXIO_nOE5-8 = 1 DIR_MIPI_AUXIO_LPC[1:8]= As required
T2	Start GPIO Signals	MIPI_AUXIO_nOE1-4 = 1 MIPI_AUXIO_nOE5-8 = 1 DIR_MIPI_AUXIO_LPC[1:8]= As required MIPI_AUXIO_LPC[1:8] = As required
T3	Enable Level Translators	MIPI_AUXIO_nOE1-4 = 0 MIPI_AUXIO_nOE5-8 = 0 DIR_MIPI_AUXIO_LPC[1:8]= As required MIPI_AUXIO_LPC[1:8] = As required

8.4. MIPI I2C Bus

Each MIPI Port connector provides a standard I2C bus to any peripheral device that may be able to use it (typically peripherals that do not utilize the MIPI BTA capability). Each connector receives its own set of SelectIO pin assignments on the FMC connector, thus there is no I2C bus sharing on either MIPI port, providing flexibility for MIPI device slave address assignment. The I2C bus of each port is IO Voltage level selectable through headers J6 for the Port A and header J17 for Port B. The jumper selection positions are identical to that of the GPIO selector headers J12 and J19, detailed earlier in Figure 8-2.

Note: The I2C translation buffer supports voltages down to VADJ=1.2V, however due to the structure of the I2C voltage translator, if the I2C bus is to be used, be aware that the I2C Port voltage level (V_MIPI_I2C_PORTx) must be configured to be at least 0.6V above that of VADJ. Examples:

1. VADJ=1.2V, then I2C Port voltage must be configured to at least 1.8V
2. VADJ=1.8V, then I2C port voltage must be configured to at least 2.5V

This voltage limitation is generally not a problem as IOStandard MIPI_DPHY_DCI requires VCCO=1.2V (reference UG571, https://www.xilinx.com/support/documentation/user_guides/ug571-ultrascale-selectio.pdf).

It is also recommended that the user review and understand the operating conditions in the I2C voltage level translator datasheet (Texas Instruments, PN: PCA9306DCUR).

The I2C translation circuit is depicted below. Note: Port A is depicted, Port B is separate, yet identical.

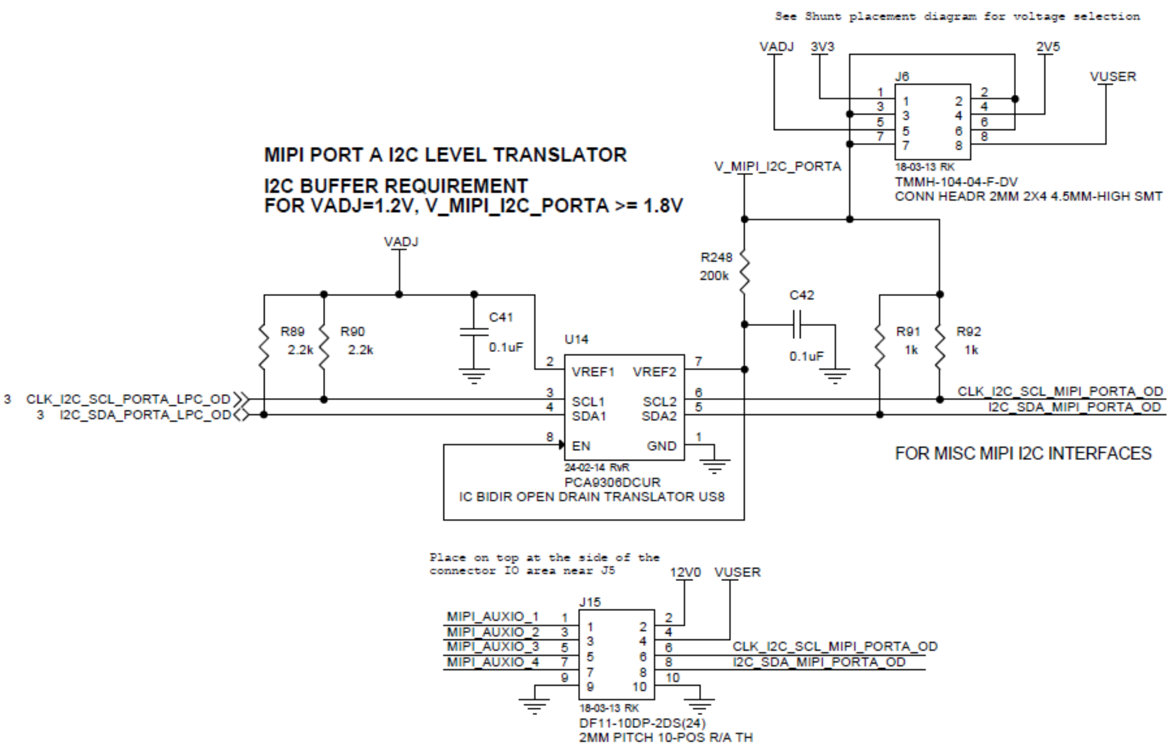


Figure 8-3 I2C Level Translation Circuitry

9. Connectors

There are three main connectors on the TB-FMCL-MIPI-DIRECT card. One LPC FMC connector (J1) provides the FMC host carrier interconnection, and the other two connectors (J5 and J16) are two right-angle MIPI port sockets facing off the front edge (I/O window) of the FMC module. Additionally, for debug and development access, two right angle headers, J15, and J18, located behind the MIPI port sockets and facing out to the board side edges, provide access to the MIPI GPIO and I2C signals as well as VUSER and 12V0.

9.1. LPC FMC Connector to Host Carrier Board

The LPC FMC connector (J1) used to mate to the Host Carrier Board is a Samtec ASP-134604-01. Only the 160-pin LPC positions are populated, however, the module may be installed on a supported HPC receptacle.

Table 9-1 shows the FMC connector pin assignment. In this table the C2M direction means Carrier-to-Mezzanine, representing an input to the FMC. The M2C direction means Mezzanine-to-Carrier, representing an output from the FMC. BIDIR identifies those signals whose direction can be application selected. Signal Direction and Description in brackets represent MIPI port option assembly. Unused LAxx, DPx, and GBTCLKx signals are not included in the table and are left unconnected. Power and GND pins are also not included; refer to Figure 3-1 for power and ground pin connections.

FPGA IO bank and pin allocations to FMC LAxx pins are platform specific and not included in the following table. Please refer to the user manual of the particular FMC host FPGA platform being used for details on the mapping of FMC IOs to FPGA banks and pins. Be aware that D-PHY capability is presently available only on HP IO pins of Xilinx UltraScale+ FPGA families. The -DIRECT card will only operate on UltraScale+ platforms where HP IOs are assigned to the FMC receptacle(s).

Table 9-1 LPC FMC Host Board Connector Pin Assignment

J1 Pin	Schematic Signal Name	VITA 57.1 Pin Name	Direction	Type	Description
MIPI HS Signals					
C14	PORTA_SLVS_HS0_P	LA10_P	BIDIR	SLVS	MIPI PORT A Channel E
C15	PORTA_SLVS_HS0_N	LA10_N			
D14	PORTA_SLVS_HS1_P	LA09_P	BIDIR	SLVS	MIPI PORT A Channel D
D15	PORTA_SLVS_HS1_N	LA09_N			
H13	PORTA_SLVS_HS2_P	LA07_P	BIDIR	SLVS	MIPI PORT A Channel C
H14	PORTA_SLVS_HS2_N	LA07_N			
G12	PORTA_SLVS_HS3_P	LA08_P	BIDIR	SLVS	MIPI PORT A Channel B
G13	PORTA_SLVS_HS3_N	LA08_N			
G6	PORTA_SLVS_HS4_P	LA00_CC_P	BIDIR	SLVS	MIPI PORT A Channel A
G7	PORTA_SLVS_HS4_N	LA00_CC_N			
H28	PORTB_SLVS_HS0_P	LA24_P	BIDIR	SLVS	MIPI PORT B Channel E
H29	PORTB_SLVS_HS0_N	LA24_N			
G27	PORTB_SLVS_HS1_P	LA25_P	BIDIR	SLVS	MIPI PORT B Channel D
G28	PORTB_SLVS_HS1_N	LA25_N			
C26	PORTB_SLVS_HS2_P	LA27_P	BIDIR	SLVS	MIPI PORT B Channel C
C27	PORTB_SLVS_HS2_N	LA27_N			
C22	PORTB_SLVS_HS3_P	LA18_CC_P	BIDIR	SLVS	MIPI PORT B

J1 Pin	Schematic Signal Name	VITA 57.1 Pin Name	Direction	Type	Description
C23	PORTB_SLVS_HS3_N	LA18_CC_N			Channel B
D20	PORTB_SLVS_HS4_P	LA17_CC_P	BIDIR	SLVS	MIPI PORT B Channel A
D21	PORTB_SLVS_HS4_N	LA17_CC_N			
MIPI GPIO and I2C Signals					
C18	MIPI_AUXIO_LPC1	LA14_P	per MIPI_AUX_DIR1	LVCMOS (VADJ)	MIPI Port A GPIO 1
C19	MIPI_AUXIO_LPC2	LA14_N	per MIPI_AUX_DIR2	LVCMOS (VADJ)	MIPI Port A GPIO 2
H19	MIPI_AUXIO_LPC3	LA15_P	per MIPI_AUX_DIR3	LVCMOS (VADJ)	MIPI Port A GPIO 3
H20	MIPI_AUXIO_LPC4	LA15_N	per MIPI_AUX_DIR4	LVCMOS (VADJ)	MIPI Port A GPIO 4
G18	MIPI_AUX_nOE1-4	LA16_P	C2M	LVCMOS (VADJ)	MIPI Port A GPIO output enable
H10	CLK_I2C_SCL_PORTA_LPC_OD	LA04_P	C2M	LVCMOS OD (VADJ)	MIPI Port A I2C Clock
H11	I2C_SDA_PORTA_LPC_OD	LA04_N	BIDIR	LVCMOS OD (VADJ)	MIPI Port A I2C Data
H31	MIPI_AUXIO_LPC5	LA28_P	per MIPI_AUX_DIR5	LVCMOS (VADJ)	MIPI Port B GPIO 1
H32	MIPI_AUXIO_LPC6	LA28_N	per MIPI_AUX_DIR6	LVCMOS (VADJ)	MIPI Port B GPIO 2
G30	MIPI_AUXIO_LPC7	LA29_P	per MIPI_AUX_DIR7	LVCMOS (VADJ)	MIPI Port B GPIO 3
G31	MIPI_AUXIO_LPC8	LA29_N	per MIPI_AUX_DIR8	LVCMOS (VADJ)	MIPI Port B GPIO 4
G19	MIPI_AUX_nOE5-8	LA16_N	C2M	LVCMOS (VADJ)	MIPI Port B GPIO output enable
H16	CLK_I2C_SCL_PORTB_LPC_OD	LA11_P	C2M	LVCMOS OD (VADJ)	MIPI Port B I2C Clock
H17	I2C_SDA_PORTB_LPC_OD	LA11_N	BIDIR	LVCMOS OD (VADJ)	MIPI Port B I2C Data
FMC Facility Signals					
C30	CLK_FMC_SCL_OD	SCL	C2M	LVTTL OD	FMC IPMI EEPROM Clk
C31	FMC_SDA_OD	SDA	BIDIR	LVTTL OD	FMC IPMI EEPROM Data
C34	GA0	GA0	C2M	LVTTL	FMC IPMI EEPROM slave address select

J1 Pin	Schematic Signal Name	VITA 57.1 Pin Name	Direction	Type	Description
					MSB
D35	GA1	GA1	C2M	LVTTL	FMC IPMI EEPROM slave address select LSB
D1	FMC_PG_C2M	PG_C2M	C2M	LVTTL	Local LDO enable
H2	GND	PRSNT_M2C_N	M2C	LVTTL	Card presence (asserted)
D30	Loop back connection	TDI	C2M	LVTTL	Looped JTAG data to maintain carrier JTAG loop
D31		TDO	M2C	LVTTL	
D29	Open	TCK	C2M	LVTTL	Not used
D33	Open	TMS	C2M	LVTTL	Not used
D34	Open	TRST_N	C2M	LVTTL	Not used
H1	TP1 testpoint	VREF_A_M2C			Testpoint access

9.2. MIPI Front Edge (I/O Window) Receptacles

The TB-FMCL-MIPI-DIRECT card utilizes Samtec Razor Beam™ LSHM series connectors for access to the MIPI ports. These 0.5mm pitch receptacles provide 40 connections in mixed differential and single-ended signals, in a format that is compact enough to fit two receptacles across a single-width FMC form-factor. Each channel connector, in addition to the 4+1 MIPI lanes, provides 12V, 3.3V, and VUSER Power (on-board selectable voltage), an I2C link, and four General Purpose IOs. Using suitable adapter modules, two MIPI camera sensors can be directly supported without need for additional external connections. The two receptacles are located side-by-side at the faceplate edge, with pinout as shown in the front view below in typical components-down orientation:

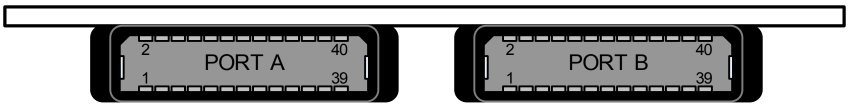


Figure 9-1 MIPI Connectors Faceplate View

Note: These connectors offer good retention force, and provide an audible notification when properly mated. During adapter insertion or extraction, "zippering" may cause irreparable damage to the connectors and/or the solder joints. It is critical that the user insert and extract mating devices in a coplanar fashion, and avoid "zippering".

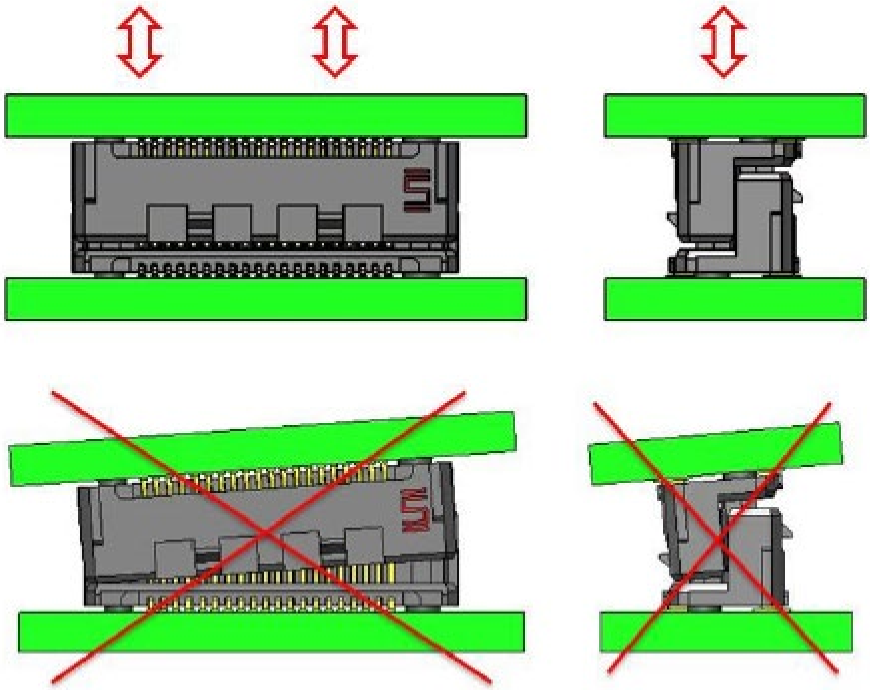


Figure 9-2 Axial removal vs zippering (picture courtesy of Samtec®)

The pinouts are provided in the following table:

Table 9-2 MIPI PORT A (J5)

Connector J5 (PORT A)				
Pin	**Signal**		**Pin**	**Signal**
1	GND		2	GND
3	NC (TEST POINT TP3)		4	PORTA_SLVS_HS4_N
5	NC (TEST POINT TP2)		6	PORTA_SLVS_HS4_P
7	GND		8	GND
9	LOOP_N		10	PORTA_SLVS_HS3_N
11	LOOP_P		12	PORTA_SLVS_HS3_P
13	GND		14	GND
15	MIPI_AUXIO_4		16	PORTA_SLVS_HS2_N
17	MIPI_AUXIO_3		18	PORTA_SLVS_HS2_P
19	GND		20	GND
21	MIPI_AUXIO_2		22	PORTA_SLVS_HS1_N
23	MIPI_AUXIO_1		24	PORTA_SLVS_HS1_P
25	GND		26	GND
27	I2C_SDA_MIPI_PORTA_OD		28	PORTA_SLVS_HS0_N
29	CLK_I2C_SCL_MIPI_PORTA_OD		30	PORTA_SLVS_HS0_P
31	GND		32	GND
33	VUSER		34	VUSER
35	GND		36	GND
37	3V3		38	3V3
39	GND		40	12V0

Notes:

- LOOP_P and LOOP_N provide a passive method for two adapters to connect. Reserved for future use.

Table 9-3 MIPI PORT B (J16)

Connector J16 (PORT B)				
Pin	**Signal**		**Pin**	**Signal**
1	GND		2	GND
3	NC (TEST POINT TP5)		4	PORTB_SLVS_HS4_N
5	NC (TEST POINT TP4)		6	PORTB_SLVS_HS4_P
7	GND		8	GND
9	LOOP_N		10	PORTB_SLVS_HS3_N
11	LOOP_P		12	PORTB_SLVS_HS3_P
13	GND		14	GND
15	MIPI_AUXIO_8		16	PORTB_SLVS_HS2_N
17	MIPI_AUXIO_7		18	PORTB_SLVS_HS2_P
19	GND		20	GND
21	MIPI_AUXIO_6		22	PORTB_SLVS_HS1_N
23	MIPI_AUXIO_5		24	PORTB_SLVS_HS1_P
25	GND		26	GND
27	I2C_SDA_MIPI_PORTB_OD		28	PORTB_SLVS_HS0_N
29	CLK_I2C_SCL_MIPI_PORTB_OD		30	PORTB_SLVS_HS0_P
31	GND		32	GND
33	VUSER		34	VUSER
35	GND		36	GND
37	3V3		38	3V3
39	GND		40	12V0

Notes:

- LOOP_P and LOOP_N provide a passive method for two adapters to connect. Reserved for future use.

9.3. MIPI GPIO and I2C Debug Headers

The MIPI debug headers are right-angle 2mm 2x5 box headers that provide access to the GPIO and I2C signals presented on the LSHM MIPI sockets. For signal integrity reasons, none of the MIPI lanes are accessible on these headers. J15 provides access to Port A control signals, and J18 provides access to Port B control signals. Both headers face out from opposite sides of the TB-FMCL-MIPI-DIRECT card and are accessible while the card is installed on a carrier provided there is nothing obstructing side access. The following figure shows the pinout order viewed from both sides of the card in the typical components-down orientation:

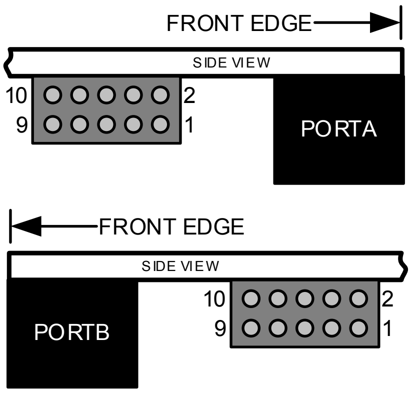


Figure 9-3 MIPI Debug header side access views

Table 9-4 MIPI GPIO Debug Headers J15 and J18

Header J15 Pin	Signal		Header J18 Pin	Signal
1	MIPI_AUXIO_1		1	MIPI_AUXIO_5
2	12V0		2	12V0
3	MIPI_AUXIO_2		3	MIPI_AUXIO_6
4	VUSER		4	VUSER
5	MIPI_AUXIO_3		5	MIPI_AUXIO_7
6	CLK_I2C_SCL_MIPI_PORTA_OD		6	CLK_I2C_SCL_MIPI_PORTB _OD
7	MIPI_AUXIO_4		7	MIPI_AUXIO_8
8	I2C_SDA_MIPI_PORTA_OD		8	I2C_SDA_MIPI_PORTB_OD
9	Ground		9	Ground
10	Ground		10	Ground

10. FMC Facility I2C Bus

10.1. FMC I2C EEPROM

A 2kbit I2C EEPROM (M24C02) is provided for FMC identification, as described in section 5.5 of ANSI/VITA 57.1. It is at I2C address 0b1010000x and is connected to the FMC dedicated I2C pins at J1-C30 (SCL) and J1-C31 (SDA). The pull-up resistors to 3V3_AUX are not populated (R148 and R149) since the pull-ups should be provided on the carrier. The EEPROM is permanently enabled for writing.

The FMC identification EEPROM is programmed at the factory to enable automated identification, verification, and configuration of Main Board parameters (typically VADJ voltage level). The contents of the EEPROM are described in Appendix A.

Note: The user must be cognizant that the FMC I2C EEPROM is always write-enabled. As it contains critical information required for correct operation, one must never overwrite the factory settings.

11. ESD Protection

All MIPI SLVS differential signals as well as the GPIO and I2C ports are protected with Texas

Instruments TPD1E05U06DPYT unidirectional ESD protection devices located close to the MIPI receptacles. They provide IEC 61000-4-2 level 4 protection and are very low capacitance (0.5pF typical) designed for up to 6Gbps speed interfaces. Applied to 100-ohm differential lines, these devices introduce less than 1dB insertion loss up to 2GHz (4Gbps).

12. Demonstration

A reference load for the ZCU102 platform is available. Please ask your sales contact for additional information.

13. Appendix A: FMC I2C EEPROM

The following table describes the contents of the FMC I2C EEPROM as programmed at the factory.

Table 13-1 FMC I2C EEPROM Contents

Board Information

Field	Size	Data
Language Code	1	0
Date / Time of Manufacture	3	<Variable>
Board Manufacturer	16	FidusSystemsInc
Board Product Name	16	TB-FMCL-MIPI-DIR
Board Serial Number	16	<Variable>
Board Part Number	16	PA-10297-01 xx=01 for Direct
FRU File ID	1	0
Hardware Revision	6	<Variable>
MAC Address	6	00:00:00:00:00:00

Multi-Record Information

VITA Subtype 0 Record

Field	Size	Data	Description
Vendor OUI	3	0x0012A2	Fixed value of 0x0012A2
Subtype/Version	1	0x00	7:4 (type): main definition type 3:0 (version): current version
Size/Connectors/Clock Dir	1	0x0C	7:6 (size): single width 5:4 (P1 size): LPC 3:2 (P2 size): not fitted 0 (clock dir): Mezzanine to Carrier 0: reserved 0
P1 Bank A Number Signals	1	0x22	34 signals
P1 Bank B Number Signals	1	0x00	
P2 Bank A Number Signals	1	0x00	
P2 Bank B Number Signals	1	0x00	
P1/P2 Number Transceivers	1	0x00	
Max Clock for TCK	1	0x95	In units of MHz: 149MHz

DC Load Record – VADJ

Field	Size	Data	Description
Output Information	1	0x00	Bit map containing output number, etc. (VADJ)
Nominal Voltage	2	0x0078	In units of 10mV (1.2V)
Minimum Voltage	2	0x0078	In units of 10mV (1.2V)
Maximum Voltage	2	0x014A	In units of 10mV (3.3V)
Ripple and Noise (PK-PK)	2	0x0032	In units of 1mV (10Hz to 30MHz) (50mV)
Minimum Current Draw	2	0x0022	In units of 1mA (34mA)
Maximum Current Draw	2	0x0064	In units of 1mA (100mA)

DC Load Record – 3P3V

Field	Size	Data	Description
Output Information	1	0x01	Bit map containing output number, etc. (3.3V)
Nominal Voltage	2	0x014A	In units of 10mV (3.3V)
Minimum Voltage	2	0x0139	In units of 10mV (3.13V)
Maximum Voltage	2	0x0154	In units of 10mV (3.4V)
Ripple and Noise (PK-PK)	2	0x0032	In units of 1mV (10Hz to 30MHz) (50mV)
Minimum Current Draw	2	0x001E	In units of 1mA (30mA)
Maximum Current Draw	2	0x0096	In units of 1mA (150mA)

DC Load Record – 12P0V

Field	Size	Data	Description
Output Information	1	0x02	Bit map containing output number, etc. (12V)
Nominal Voltage	2	0x04B0	In units of 10mV (12V)
Minimum Voltage	2	0x0474	In units of 10mV (11.4V)
Maximum Voltage	2	0x04EC	In units of 10mV (12.6V)
Ripple and Noise (PK-PK)	2	0x0064	In units of 1mV (10Hz to 30MHz) (100mV)
Minimum Current Draw	2	0x0023	In units of 1mA (35mA)
Maximum Current Draw	2	0x01F4	In units of 1mA (500mA)

DC Output Record – VIO_B_M2C (DOES NOT EXIST, LPC)

Field	Size	Data	Description
Output Information	1	0x03	Bit map containing output number, etc.
Nominal Voltage	2	0x0000	In units of 10mV
Minimum Voltage	2	0x0000	In units of 10mV
Maximum Voltage	2	0x0000	In units of 10mV
Ripple and Noise (PK-PK)	2	0x0000	In units of 1mV (10Hz to 30MHz)
Minimum Current Load	2	0x0000	In units of 1mA
Maximum Current Load	2	0x0000	In units of 1mA

DC Output Record – VREF_A_M2C (NOT CONNECTED)

Field	Size	Data	Description
Output Information	1	0x04	Bit map containing output number, etc.
Nominal Voltage	2	0x0000	In units of 10mV
Minimum Voltage	2	0x0000	In units of 10mV
Maximum Voltage	2	0x0000	In units of 10mV
Ripple and Noise (PK-PK)	2	0x0000	In units of 1mV (10Hz to 30MHz)
Minimum Current Load	2	0x0000	In units of 1mA
Maximum Current Load	2	0x0000	In units of 1mA

DC Output Record – VREF_B_M2C (DOES NOT EXIST, LPC)

Field	Size	Data	Description
Output Information	1	0x05	Bit map containing output number, etc.
Nominal Voltage	2	0x0000	In units of 10mV
Minimum Voltage	2	0x0000	In units of 10mV
Maximum Voltage	2	0x0000	In units of 10mV
Ripple and Noise (PK-PK)	2	0x0000	In units of 1mV (10Hz to 30MHz)
Minimum Current Load	2	0x0000	In units of 1mA
Maximum Current Load	2	0x0000	In units of 1mA

14. Appendix B: Headers, Factory Default, and Orientation

The following depicts the factory default header jumper positions and clarifies the pin numbering and orientation of the headers. Default strap selected functions are as follows:

Table 14-1 Default Header Explanation

Option Header	Function Selected
J6	7-8: MIPI PORT A I2C set to VUSER IO voltage
J9	5-6: VUSER set to 1.8V
J12	7-8: MIPI PORT A MIPI_AUXIO_(1-4) set to VUSER IO voltage
J17	7-8: MIPI PORT B I2C set to VUSER IO voltage
J19	7-8: MIPI PORT B MIPI_AUXIO_(5-8) set to VUSER IO voltage

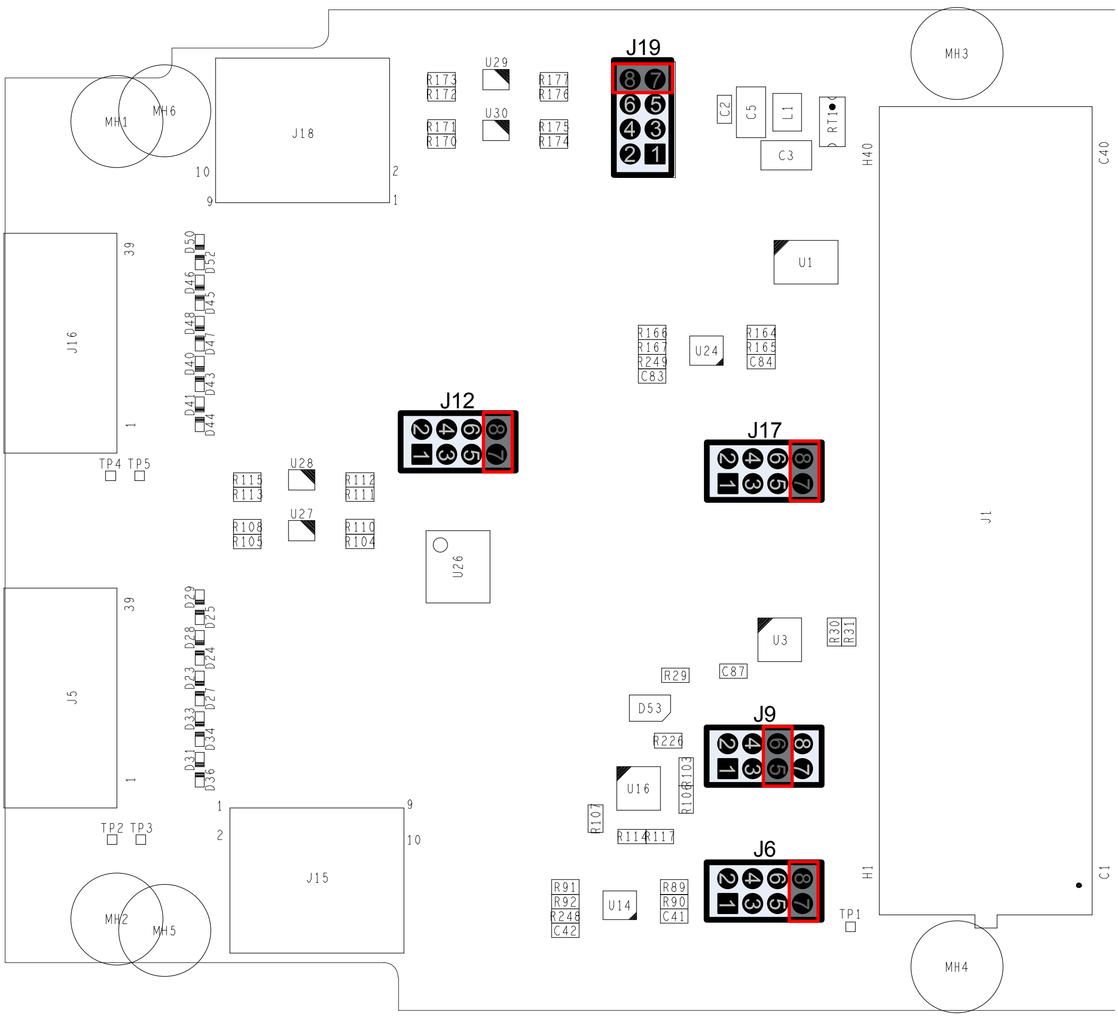


Figure 14-1 Default Jumper Positions and Header Orientation

™ TOKYO ELECTRON DEVICE

URL: http://solutions.inrevium.com/
http://solutions.inrevium.com/jp/
E-mail: psd-sales@teldevice.co.jp

HEAD Quarter: Yokohama East Square, 1-4 Kinko-cho, Kanagawa-ku, Yokohama City,
Kanagawa, Japan 221-0056
TEL: +81-45-443-4031 FAX: +81-45-443-4063