

## LVPECL, LVDS, and HCSL Crystal Oscillator

### Features

- 40 fs<sub>RMS</sub> Phase Jitter Typical, 12 kHz to 20 MHz
- 3rd OT or Fundamental Crystal Design
- Extended Operating Temperature Range: -55°C to +125°C
- 100 MHz to 320 MHz Output Frequencies
- Excellent Power Supply Rejection Ratio
- Glitch Free Output upon Power-Up and Enable
- Hermetically Sealed 3.2 mm × 2.5 mm Ceramic Package
- Product is Compliant to RoHS Directive and Fully Compatible with Lead-Free Assembly

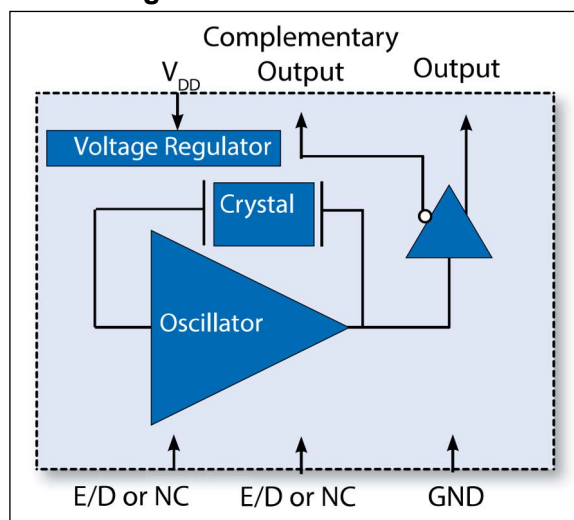
### Applications

- Medical, Ultrasound
- Ethernet, GbE, SynchE
- Fibre Channel
- PON
- Clock Source for A/Ds, D/As, FPGAs
- Test and Measurement
- Storage Area Network

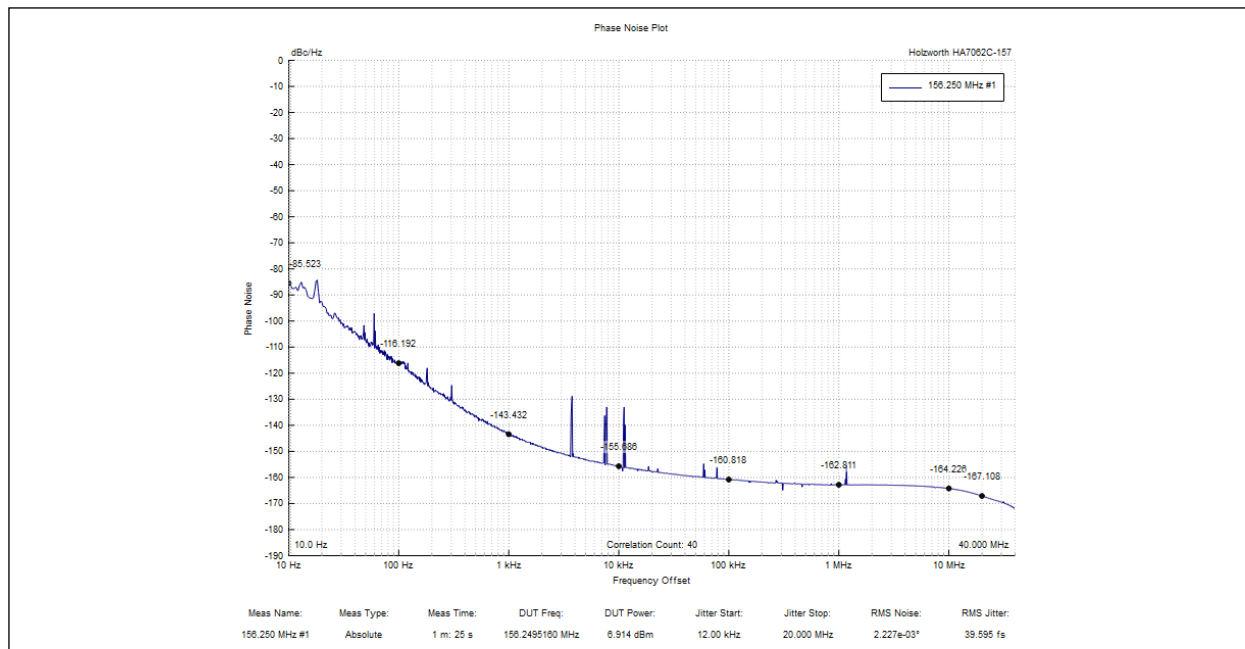
### General Description

Microchip's VC-830 crystal oscillator is a quartz-stabilized, differential output oscillator that operates off a 1.8V, 2.5V, or 3.3V power supply in a hermetically sealed 3.2 mm × 2.5 mm ceramic package.

### Block Diagram



### Phase Noise Plot



**FIGURE 0-1:** RMS Jitter, 40 fs<sub>RMS</sub> at 156.25 MHz, over 12 kHz to 20 MHz.

# VC-830

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Supply Voltage .....	-0.3V to +4.5V
Enable/Disable Voltage .....	-0.3V to $V_{DD} + 0.3V$
ESD Rating, Human Body Model (Note 1) .....	2 kV
ESD Rating, Charged Device Model (Note 1) .....	200V
Storage Temperature ( $T_S$ ) .....	-55°C to +125°C
Junction Temperature ( $T_J$ ) .....	+150°C

† **Notice:** Stresses in excess of the Absolute Maximum Ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to Absolute Maximum Ratings for extended periods may adversely affect device reliability.

**Note 1:** Although ESD protection circuitry has been designed into the VC-830, proper precautions should be taken when handling and mounting. Microchip employs a Human Body Model (HBM) and a Charged Device Model (CDM) for ESD susceptibility testing and design protection evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry standard has been adopted for the CDM, a standard resistance of 1.5 k $\Omega$  and capacitance of 100 pF is widely used and therefore can be used for comparison purposes.

### ELECTRICAL CHARACTERISTICS, LVPECL OPTION

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage (Note 1)	$V_{DD}$	2.375	2.5	2.625	V	Ordering Option
		3.135	3.3	3.465		
Current Consumption	$I_{DD}$	—	—	66	mA	200 MHz
		—	—	70		320 MHz
<b>Frequency</b>						
Nominal Frequency	$f_N$	100	—	320	MHz	Ordering Option
Stability (Note 2)	—	—	—	$\pm 20$	ppm	Ordering Option
		—	—	$\pm 25$		
		—	—	$\pm 30$		
		—	—	$\pm 50$		
		—	—	$\pm 100$		
<b>Outputs</b>						
Output Logic Level High (Note 3)	$V_{OH}$	$V_{DD} - 1.085$	—	$V_{DD} - 0.880$	V	$V_{DD} = +2.5V$
Output Logic Level Low (Note 3)	$V_{OL}$	$V_{DD} - 1.810$	—	$V_{DD} - 1.620$		

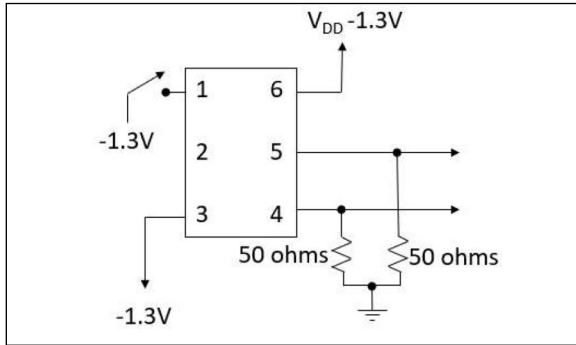
- Note 1:** The VC-830 power supply should be filtered. For example, a 10  $\mu F$ , 0.1  $\mu F$ , and 0.01  $\mu F$  capacitor.
- Note 2:** Includes calibration tolerance, operating temperature, supply voltage variations, aging, and IR reflow.
- Note 3:** Figure 1-1 defines the test circuit and Figure 1-2 defines these parameters.
- Note 4:** Output rise and fall time will be 600 ps (max.) for -40°C to +105°C, -40°C to +125°C, and -55°C to +125°C operating temperature ranges.
- Note 5:** Duty Cycle is measured as On/Time Period.
- Note 6:** Measured using an Agilent E5052 Signal Source Analyzer at 25°C.
- Note 7:** Outputs will be enabled if Enable/Disable is left open. There is an oscillation detection circuit that ensures glitch free output upon power-up or enable.
- Note 8:** In order to reduce current, the pull-up resistance is higher when  $V_{DD}$  is set to ground.

## ELECTRICAL CHARACTERISTICS, LVPECL OPTION (CONTINUED)

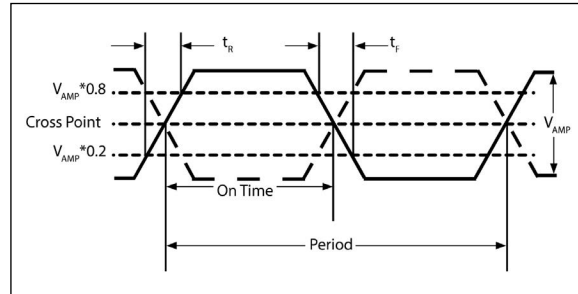
Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Output Logic Level High (Note 3)	$V_{OH}$	$V_{DD} - 1.085$	—	$V_{DD} - 0.880$	V	$V_{DD} = +3.3V$
Output Logic Level Low (Note 3)	$V_{OL}$	$V_{DD} - 1.810$	—	$V_{DD} - 1.620$		
Output Rise and Fall Time (Note 3)	$t_r/t_f$	—	—	400	ps	Note 4
Load	—	50 $\Omega$ into $V_{DD} - 2.0V$			—	—
Duty Cycle (Note 5)	DC	45	—	55	%	—
Phase Noise, 3.3V, 156.25 MHz (Note 6)	$\phi_N$	—	-79	—	dBc/Hz	10 Hz
		—	-110	—		100 Hz
		—	-130	—		1 kHz
		—	-154	—		10 kHz
		—	-160	—		100 kHz
		—	-163	—		1 MHz
		—	-163	—		10 MHz
—	-167	—	20 MHz			
Phase Jitter, 156.25 MHz, 12 kHz to 20 MHz (Note 6)	$\phi_J$	—	40	60	fs	—
<b>Enable/Disable</b>						
Outputs Enabled (Note 7)	$V_{IH}$	$0.7 * V_{DD}$	—	—	V	—
Outputs Disabled	$V_{IL}$	—	—	$0.3 * V_{DD}$	V	—
Disable Time	$t_D$	—	—	200	ns	—
E/D Pull-Up Resistance (Note 8)	—	0.5	—	2	M $\Omega$	E/D = GND
E/D Pull-Up Resistance	—	30	—	150	k $\Omega$	E/D = $V_{DD}$
Start-Up Time	$t_{SU}$	—	—	10	ms	—
Operating Temperature	$T_{OP}$	-10	—	70	°C	Ordering Option
		-40	—	85		
		-40	—	105		
		-40	—	125		
		-55	—	125		

- Note 1:** The VC-830 power supply should be filtered. For example, a 10  $\mu F$ , 0.1  $\mu F$ , and 0.01  $\mu F$  capacitor.
- Note 2:** Includes calibration tolerance, operating temperature, supply voltage variations, aging, and IR reflow.
- Note 3:** Figure 1-1 defines the test circuit and Figure 1-2 defines these parameters.
- Note 4:** Output rise and fall time will be 600 ps (max.) for  $-40^\circ C$  to  $+105^\circ C$ ,  $-40^\circ C$  to  $+125^\circ C$ , and  $-55^\circ C$  to  $+125^\circ C$  operating temperature ranges.
- Note 5:** Duty Cycle is measured as On/Time Period.
- Note 6:** Measured using an Agilent E5052 Signal Source Analyzer at  $25^\circ C$ .
- Note 7:** Outputs will be enabled if Enable/Disable is left open. There is an oscillation detection circuit that ensures glitch free output upon power-up or enable.
- Note 8:** In order to reduce current, the pull-up resistance is higher when  $V_{DD}$  is set to ground.

# VC-830



**FIGURE 1-1:** LVPECL Test Circuit.



**FIGURE 1-2:** LVPECL Output Rise/Fall Time.

## ELECTRICAL CHARACTERISTICS, LVDS OPTION

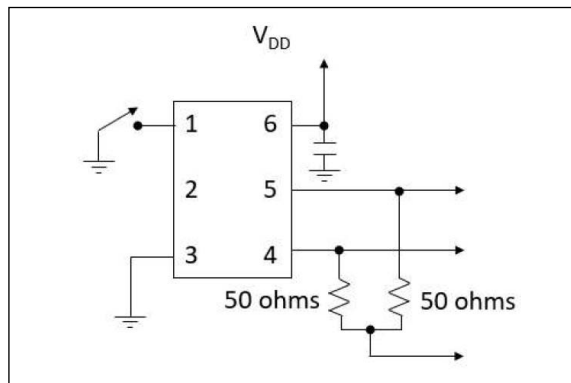
Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage (Note 1)	$V_{DD}$	1.71	1.8	1.89	V	Ordering Option
		2.37	2.5	2.625		
		3.135	3.3	3.465		
Current Consumption	$I_{DD}$	—	—	25	mA	1.8V, 175 MHz
		—	—	29		2.5V, 200 MHz
		—	—	35		2.5V, 320 MHz
		—	—	30		3.3V, 200 MHz
		—	—	35		3.3V, 320 MHz
<b>Frequency</b>						
Nominal Frequency	$f_N$	100	—	320	MHz	Ordering Option, Note 9
Stability (Note 2)	—	—	—	±20	ppm	Ordering Option
		—	—	±25		
		—	—	±30		
		—	—	±50		
		—	—	±100		
<b>Outputs</b>						
Output Logic Level High (Note 3)	$V_{OH}$	—	1.43	1.6	V	—
Output Logic Level Low (Note 3)	$V_{OL}$	0.9	1.10	—		
Differential Output Amplitude	—	247	350	454	mV	100Ω Differential load

- Note 1:** The VC-830 power supply should be filtered. For example, a 10  $\mu$ F, 0.1  $\mu$ F, and 0.01  $\mu$ F capacitor.
- Note 2:** Includes calibration tolerance, operating temperature, supply voltage variations, aging, and IR reflow.
- Note 3:** Figure 1-3 defines the test circuit and Figure 1-2 defines these parameters.
- Note 4:** Output rise and fall time will be 600 ps (max.) for  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  operating temperature ranges.
- Note 5:** Duty Cycle is measured as On/Time Period.
- Note 6:** Measured using an Agilent E5052 Signal Source Analyzer at  $25^{\circ}\text{C}$ .
- Note 7:** Outputs will be enabled if Enable/Disable is left open. There is an oscillation detection circuit that ensures glitch free output upon power-up or enable.
- Note 8:** In order to reduce current, the pull-up resistance is higher when  $V_{DD}$  is set to ground.
- Note 9:** 1.8V option available up to 175 MHz.

## ELECTRICAL CHARACTERISTICS, LVDS OPTION (CONTINUED)

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Differential Output Error	—	—	—	50	mV	—
Offset Voltage	—	1.125	1.25	1.375	V	—
Offset Voltage Error	—	—	—	50	mV	—
Output Leakage Current, Outputs Disabled	—	—	—	30	μA	—
Output Rise and Fall Time (Note 3)	$t_r/t_f$	—	—	300	ps	Note 4
Load	—	100Ω Differential			—	—
Duty Cycle (Note 5)	DC	45	—	55	%	—
Phase Noise, 3.3V, 156.25 MHz (Note 6)	$\phi_N$	—	-79	—	dBc/Hz	10 Hz
		—	-110	—		100 Hz
		—	-130	—		1 kHz
		—	-154	—		10 kHz
		—	-160	—		100 kHz
		—	-162	—		1 MHz
		—	-163	—		10 MHz
		—	-164	—		20 MHz
Phase Jitter, 156.25 MHz, 12 kHz to 20 MHz (Note 6)	$\phi_J$	—	43	64	fs	—
<b>Enable/Disable</b>						
Outputs Enabled (Note 7)	$V_{IH}$	$0.7 * V_{DD}$	—	—	V	—
Outputs Disabled	$V_{IL}$	—	—	$0.3 * V_{DD}$	V	—
Disable Time	$t_D$	—	—	200	ns	—
E/D Pull-Up Resistance (Note 8)	—	0.5	—	2	MΩ	E/D = GND
E/D Pull-Up Resistance	—	30	—	150	kΩ	E/D = $V_{DD}$
Start-Up Time	$t_{SU}$	—	—	10	ms	—
Operating Temperature	$T_{OP}$	-10	—	70	°C	Ordering Option
		-40	—	85		
		-40	—	105		
		-40	—	125		
		-55	—	125		

- Note 1:** The VC-830 power supply should be filtered. For example, a 10 μF, 0.1 μF, and 0.01 μF capacitor.
- 2:** Includes calibration tolerance, operating temperature, supply voltage variations, aging, and IR reflow.
- 3:** Figure 1-3 defines the test circuit and Figure 1-2 defines these parameters.
- 4:** Output rise and fall time will be 600 ps (max.) for -40°C to +105°C, -40°C to +125°C, and -55°C to +125°C operating temperature ranges.
- 5:** Duty Cycle is measured as On/Time Period.
- 6:** Measured using an Agilent E5052 Signal Source Analyzer at 25°C.
- 7:** Outputs will be enabled if Enable/Disable is left open. There is an oscillation detection circuit that ensures glitch free output upon power-up or enable.
- 8:** In order to reduce current, the pull-up resistance is higher when  $V_{DD}$  is set to ground.
- 9:** 1.8V option available up to 175 MHz.



**FIGURE 1-3:** LVDS Test Circuit.

## ELECTRICAL CHARACTERISTICS, HCSL OPTION

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage (Note 1)	$V_{DD}$	1.71	1.8	1.81	V	Ordering Option
		2.375	2.5	2.625		
		3.135	3.3	3.465		
Current Consumption	$I_{DD}$	—	—	46	mA	1.8V: 175 MHz 2.5V, 3.3V: 200 MHz
		—	—	53		1.8V, 2.5V, 3.3V, 312 MHz
<b>Frequency</b>						
Nominal Frequency	$f_N$	100	—	312	MHz	Ordering Option, Note 8
Stability (Note 2)	—	—	—	±20	ppm	Ordering Option
		—	—	±25		
		—	—	±30		
		—	—	±50		
		—	—	±100		
<b>Outputs</b>						
Output Logic Level High (Note 3)	$V_{OH}$	0.55	—	1.0	V	1.8V
		0.6	—	0.9		2.5V, 3.3V
Output Logic Level Low (Note 3)	$V_{OL}$	-0.15	—	0.15		—
Output Leakage Current, Outputs Disabled	—	—	—	30	μA	—
Output Rise and Fall Time (Note 3)	$t_r/t_f$	—	—	600	ps	—

- Note 1:** The VC-830 power supply should be filtered. For example, a 10 μF, 0.1 μF, and 0.01 μF capacitor.
- Note 2:** Includes calibration tolerance, operating temperature, supply voltage variations, aging, and IR reflow.
- Note 3:** Figure 1-3 defines the test circuit and Figure 1-2 defines these parameters.
- Note 4:** Duty Cycle is measured as On/Time Period.
- Note 5:** Measured using an Agilent E5052 Signal Source Analyzer at 25°C.
- Note 6:** Outputs will be enabled if Enable/Disable is left open. There is an oscillation detection circuit that ensures glitch free output upon power-up or enable.
- Note 7:** In order to reduce current, the pull-up resistance is higher when  $V_{DD}$  is set to ground.
- Note 8:** 1.8V option available up to 175 MHz.

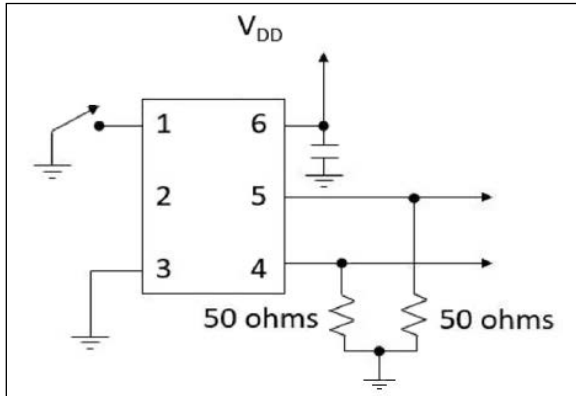
## ELECTRICAL CHARACTERISTICS, HCSL OPTION (CONTINUED)

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Load	—	50Ω to GND			—	—
Duty Cycle (Note 4)	DC	45	—	55	%	—
Phase Noise, 3.3V, 156.25 MHz (Note 5)	$\phi_N$	—	-79	—	dBc/Hz	10 Hz
		—	-110	—		100 Hz
		—	-130	—		1 kHz
		—	-154	—		10 kHz
		—	-160	—		100 kHz
		—	-162	—		1 MHz
		—	-163	—		10 MHz
Phase Jitter, 100.000 MHz, 12 kHz to 20 MHz (Note 5)	$\phi_J$	—	55	—	fs	—
<b>Enable/Disable</b>						
Outputs Enabled (Note 6)	$V_{IH}$	$0.7 * V_{DD}$	—	—	V	—
Outputs Disabled	$V_{IL}$	—	—	$0.3 * V_{DD}$	V	—
Disable Time	$t_D$	—	—	200	ns	—
E/D Pull-Up Resistance (Note 7)	—	0.5	—	2	MΩ	E/D = GND
E/D Pull-Up Resistance	—	30	—	150	kΩ	E/D = $V_{DD}$
Start-Up Time	$t_{SU}$	—	—	10	ms	—
Operating Temperature	$T_{OP}$	-10	—	70	°C	Ordering Option
		-40	—	85		
		-40	—	105		
		-40	—	125		
		-55	—	125		

- Note 1:** The VC-830 power supply should be filtered. For example, a 10 μF, 0.1 μF, and 0.01 μF capacitor.
- Note 2:** Includes calibration tolerance, operating temperature, supply voltage variations, aging, and IR reflow.
- Note 3:** Figure 1-3 defines the test circuit and Figure 1-2 defines these parameters.
- Note 4:** Duty Cycle is measured as On/Time Period.
- Note 5:** Measured using an Agilent E5052 Signal Source Analyzer at 25°C.
- Note 6:** Outputs will be enabled if Enable/Disable is left open. There is an oscillation detection circuit that ensures glitch free output upon power-up or enable.
- Note 7:** In order to reduce current, the pull-up resistance is higher when  $V_{DD}$  is set to ground.
- Note 8:** 1.8V option available up to 175 MHz.

# VC-830

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**FIGURE 1-4:** HCSL Test Circuit.

## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 2-1](#).

**TABLE 2-1: PIN FUNCTION TABLE**

Pin Number	Pin Name	Description
1	E/D or NC	Enable/Disable or No Connect.
2	E/D or NC	Enable/Disable or No Connect.
3	GND	Electrical and lid ground.
4	$f_O$	Output frequency.
5	$Cf_O$	Complementary output frequency.
6	$V_{DD}$	Supply voltage.

**Note:** Pin 2 can be E/D and Pin 1 will be NC. Use Ordering Option B.

**TABLE 2-2: ENABLE/DISABLE FUNCTION**

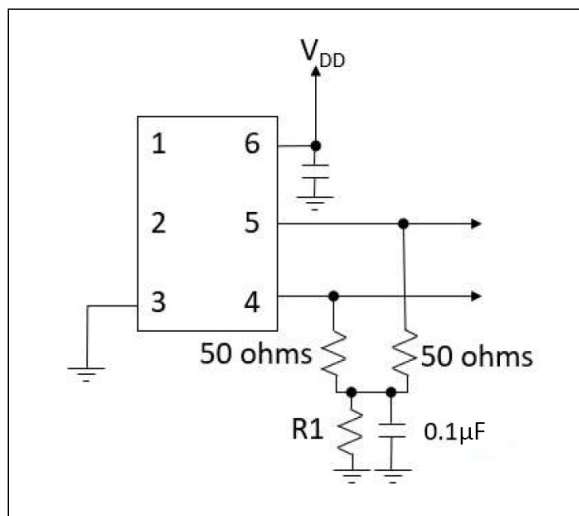
E/D Pin	Output
High	Clock Output
Open	Clock Output
Low	High Impedance

## 3.0 APPLICATION DIAGRAMS

### 3.1 LVPECL Application Diagrams

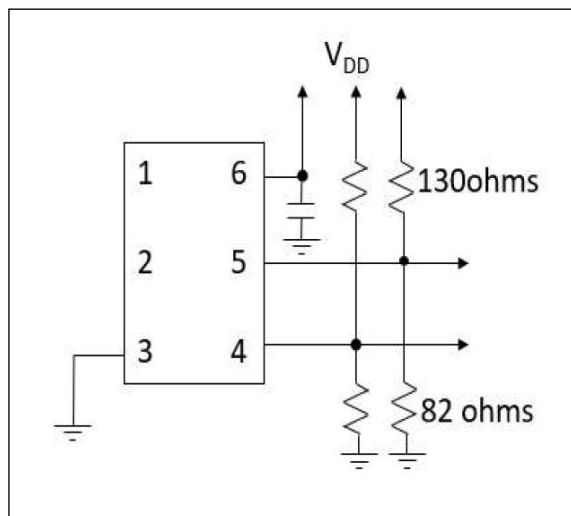
The VC-830 incorporates a standard LVPECL output scheme, which are unterminated FET drains. There are numerous application notes on terminating and interfacing LVPECL logic and the two most common methods are a single resistor to ground (Figure 3-1) and a pull-up/pull-down scheme as shown in Figure 3-2. AC-coupling capacitors are optional, depending on the application and the input logic requirements of the next stage.

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left unterminated because if one of the two outputs is left open, it will result in excessive jitter on both. PCB layout must take this and 50Ω impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.



**FIGURE 3-1:** LVPECL Pull-Down Resistor Termination Scheme.

Figure 3-1 shows one option to terminate LVPECL outputs and is optimized to reduce common mode noise. R1 is 50Ω for 3.3V supply voltage and 18Ω for 2.5V.

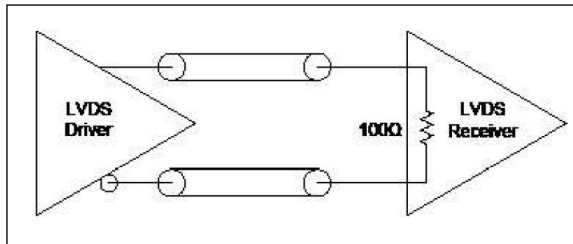


**FIGURE 3-2:** LVPECL Pull-Up/Pull-Down Termination.

Resistor values shown are typical for 3.3V operation. For 2.5V operation, the resistor to ground is 62Ω and the resistor to supply is 250Ω.

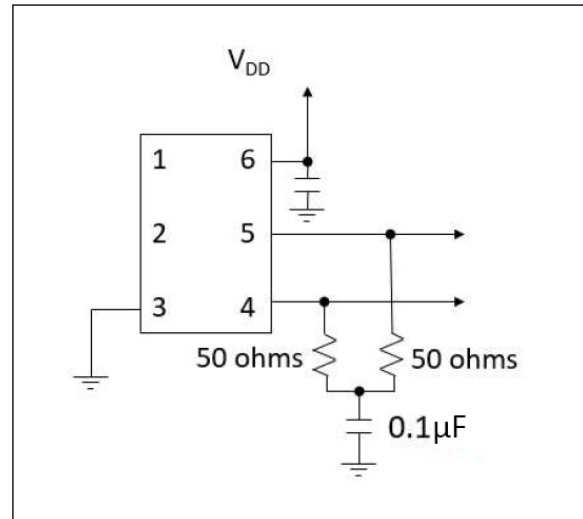
### 3.2 LVDS Application Diagrams

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left unterminated because if one of the two outputs is left open, it will result in excessive jitter on both. PCB layout must take this and 50Ω impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.



**FIGURE 3-3:** LVDS-to-LVDS Connection, Internal 100Ω Resistor.

Some LVDS structures have an internal 100Ω resistor on the input and do not need additional components. AC blocking capacitors can be used if the DC levels are incompatible.



**FIGURE 3-4:** LVDS-to-LVDS Connection.

Some input structures may not have an internal 100Ω resistor on the input and will need an external 100Ω resistor located at the receiver for impedance matching. Figure 3-4 is optimized to reduce common mode noise. Additionally, the input may have an internal DC bias that may not be compatible with LVDS levels. AC blocking capacitors, such as 0.1 μF, should be used in this case.

## 4.0 RELIABILITY

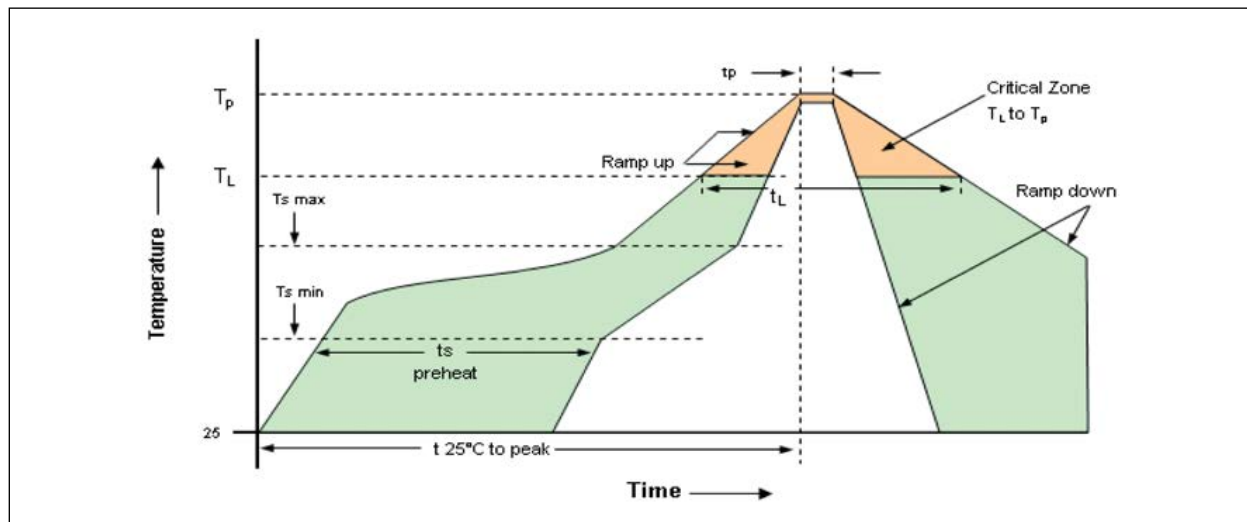
Microchip qualification will include aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VC-830 family is capable of meeting the following qualification tests.

**TABLE 4-1: ENVIRONMENTAL COMPLIANCE**

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Temperature Cycle	MIL-STD-883, Method 1010
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2015
Moisture Sensitivity Level	MSL 1
Contact Pads	Gold (0.3 $\mu\text{m}$ min., 1.0 $\mu\text{m}$ max.) over Nickel
$\theta_{\text{JC}}$ (Bottom of Case)	28°C/W
Maximum Junction Temperature	150°C
Weight	23 mg

## 5.0 IR REFLOW

Devices are built using lead-free epoxy and can be subjected to standard lead-free IR reflow conditions shown in [Table 5-1](#). Contact pads are gold over nickel and lower maximum temperatures can also be used, such as 220°C.



**FIGURE 5-1:** Reflow Solder Profile.

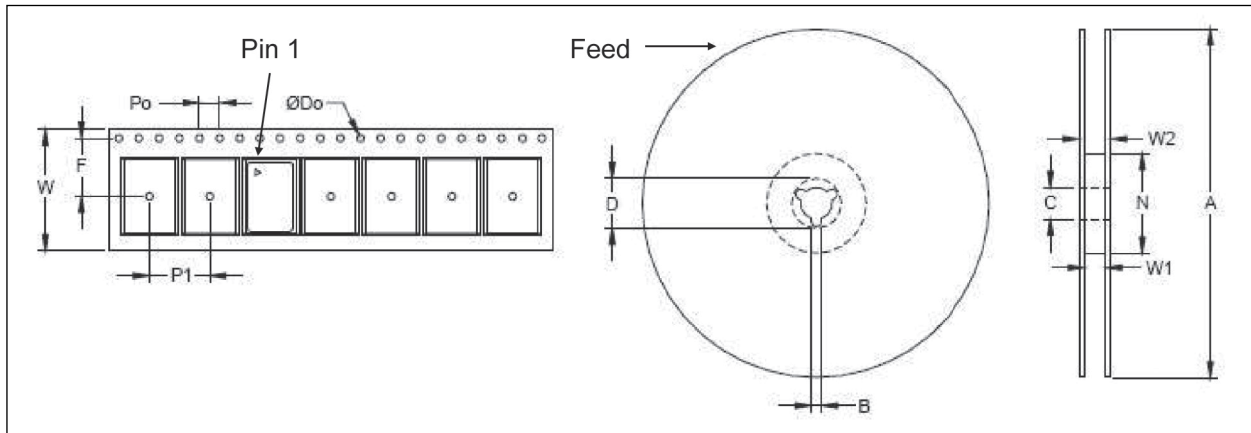
**TABLE 5-1: REFLOW PROFILE**

Parameter	Symbol	Value
Pre-Heat Time	$t_S$	200 seconds maximum
Ramp Up	$R_{UP}$	3°C/sec. maximum
Time above 217°C	$t_L$	150 seconds maximum
Time to Peak Temperature	$T_{AMB-P}$	480 seconds maximum
Time at 260°C	$t_P$	30 seconds maximum
Time at 240°C	$t_{P2}$	60 seconds maximum
Ramp Down	$R_{DN}$	6°C/sec. maximum

## 6.0 TAPE AND REEL

**TABLE 6-1: TAPE AND REEL DIMENSIONS**

Tape Dimensions (mm)						Reel Dimensions (mm)							
Dimension	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	# per Reel
Tolerance	Typ	Typ	Typ	Typ	Typ	Typ	Typ	Typ	Typ	Typ	Typ	Max	
VC-830	8	3.5	1.5	4	4	178	2	13	21	60	10	14	3000



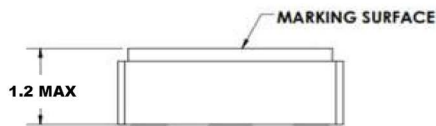
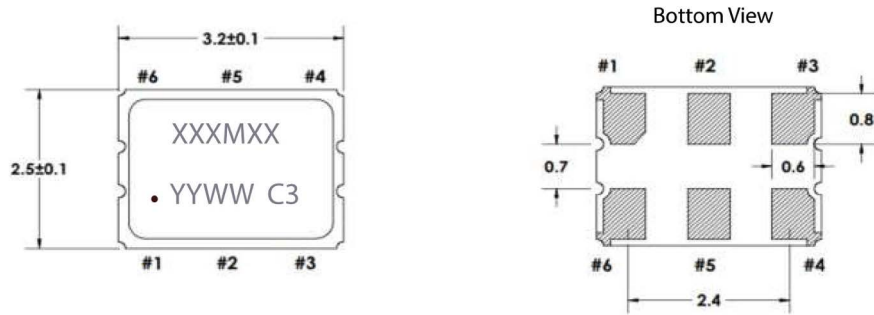
**FIGURE 6-1:** Tape and Reel Diagram.

# VC-830

## 7.0 PACKAGING INFORMATION

### 6-Lead 3.2 mm × 2.5 mm Package Outline and Recommended Land Pattern

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



#### Marking Information:

XXXMXX = Frequency (example: 100M00)

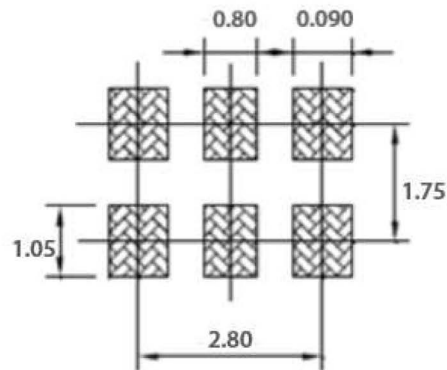
YY = Year of Manufacture

WW = Week of the Year

C3 = Manufacturing Location

• = Pin 1 Indicator

Dimensions in mm



## APPENDIX A: REVISION HISTORY

### Revision A (May 2021)

- Converted Vectron document VC-830 to Microchip data sheet template DS20006510A.
- Minor grammatical text changes throughout.

### Revision B (August 2021)

- Added a plus/minus ( $\pm$ ) symbol to each value listed for Output Amplitude in the [Electrical Characteristics, LVDS Option](#) table.
- Updated maximum package height to 1.2 mm.

### Revision C (April 2024)

- Corrected the Storage Temperature range in the Absolute Maximum Ratings section.
- Added new HCSL ordering option details throughout document, including but not limited to the [Electrical Characteristics, HCSL Option](#), table and [Figure 1-4](#).

### Revision D (December 2024)

- Updated [Features](#).
- Updated [Electrical Characteristics, LVPECL Option](#), [Electrical Characteristics, LVDS Option](#), and [Electrical Characteristics, HCSL Option](#).
- Updated the [Product Identification System](#) section.

# VC-830

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## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>Device</u>	<u>-X</u>	<u>X</u>	<u>X</u>	<u>-X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>-XXXXXXXXXX</u>	<u>XX</u>
Part No.	Power Supply	Output	Temp. Range	Stability	E/D Logic	E/D Pin	Custom Options	Frequency	Packaging
<b>Device:</b>	VC-830:	LVPECL, LVDS Crystal Oscillator in 6-Lead 3.2 mm x 2.5 mm VDFN							
<b>Power Supply:</b>	E =	3.3VDC ±5%							
	H =	2.5VDC ±5%							
	J =	1.8VDC ±5%							
<b>Output:</b>	C =	LVPECL							
	D =	LVDS							
	H =	HCSL							
<b>Temperature Range:</b>	E =	-40°C to +85°C							
	F =	-40°C to +105°C							
	W =	-10°C to +70°C							
	G =	-40°C to +125°C							
	C =	-55°C to +125°C							
<b>Stability:</b>	E =	±20 ppm							
	F =	±25 ppm							
	G =	±30 ppm							
	K =	±50 ppm							
	S =	±100 ppm							
<b>Enable/Disable Logic:</b>	A =	Output Enabled with a Logic High or Open							
<b>Enable/Disable Pin:</b>	A =	Pin 1 (Pin 2 = No Connect)							
	B =	Pin 2 (Pin 1 = No Connect)							
<b>Custom Options:</b>	N =	Standard option							
<b>Frequency:</b>	xxxMxxxxx=Frequency in MHz								
<b>Packaging:</b>	TR =	3,000/Reel							
	<blank>=	Cut Tape/ non-TR quantities							
<b>Examples:</b>									
a) VC-830-ECF-GAAN-156M250000TR: VC-830, 3.3VDC, LVPECL Output, -40°C to +105°C Temp Range, ±30 ppm Stability, Output Enabled, Pin 1 Enable/Disable, Standard Option, 156.25 MHz, 3000/Reel									
b) VC-830-HDW-KAAN-125M000000TR: VC-830, 2.5VDC, LVDS Output, -10°C to +70°C Temp Range, ±50 ppm Stability, Output Enabled, Pin 1 Enable/Disable, Standard Option, 125 MHz, 3000/Reel									
<b>Note 1:</b> Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.									

**Note:** Not all combinations of options are available. Other specifications may be available upon request.

# VC-830

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