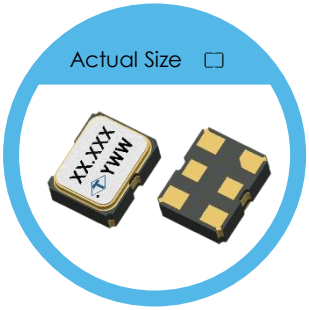
TAITIEN
Our Performance, Your Reputation

OB Type

2.5 x 2.0 mm SMD Differential Output Crystal Oscillator



RoHS Compliant

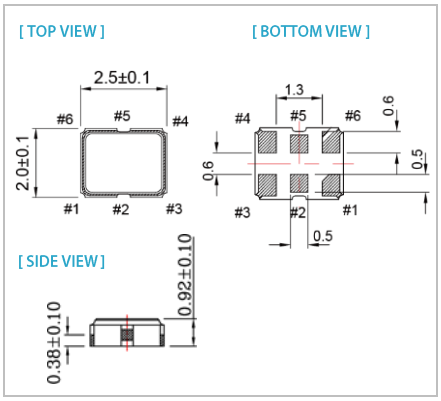
FEATURES

- Industry Standard 2.5 x 2.0 x 0.92mm Hermetically Sealed Ceramic Package
- Low Jitter Performance: Typical 0.15pS RMS from 12kHz - 20MHz
- Fundamental/3rd Overtone Crystal Design
- Output Frequency up to 220MHz
- Tri-State Enable/Disable

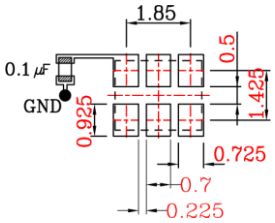
TYPICAL APPLICATION

- 10Gbit Ethernet, Fiber Channel, Storage Area Network, SONET
- Enterprise Servers, Reference Clocks for ADC and DAC, Telecom

DIMENSION (mm)



SOLDER PAD LAYOUT (mm)



To ensure optimal oscillator performance, place a by-pass capacitor of 0.1μF as close to the part as possible between V_{DD} and GND pads.

PIN FUNCTION (mm)

PIN#	FUNCTION
1	NC/Tri-State
2	Tri-State/NC
3	GND
4	Output
5	Comp. Output
6	V_{DD}

ELECTRICAL SPECIFICATION

Parameter		LVPECL				Unit	Test Condition
		3.3V		2.5V			
		Min.	Max.	Min.	Max.		
Supply Voltage Variation (V_{DD})		V_{DD} – 10%	V_{DD} + 10%	V_{DD} – 5%	V_{DD} + 5%	V	
Frequency Range		13.5	220	13.5	220	MHz	
Standard Frequency		100, 125, 156.25				MHz	Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.
Power Current Consumption			55		55	mA	
Output Level	Output High	2.215	2.42	1.415	1.64	V	
	Output Low	1.49	1.68	0.69	0.88	V	
Transition Time	Rise Time		0.6		0.6	nSec	Transition times are measured between 20% and 80%
	Fall Time		0.6		0.6	nSec	
Duty Cycle		45	55	45	55	%	
Startup Time			10		10	mSec	
Tri-State	Enable	0.7 x V_{DD}		0.7 x V_{DD}		V	
	Disable		0.3 x V_{DD}		0.3 x V_{DD}	V	
Stand by Current			30		30	μA	
Output Loading		50Ω, V_{DD} – 2V					
RMS Phase Jitter Integrated 12 kHz~20 MHz @ 3.3V	13.5MHz~80MHz		1		1	pSec	
	80MHz~220MHz		0.3		0.3	pSec	
Aging (@ 25°C, First Year)			±3		±3	ppm	
Storage Temp. Range		-55	125	-55	125	°C	
Phase Noise		Typ.	Max.	Typ.	Max.		
At V_{DD}=3.3V, fout=156.25MHz	10kHz offset	-143		-145		dBc/Hz	
	100kHz offset	-151		-154		dBc/Hz	
	1MHz offset	-155		-155		dBc/Hz	

Note: not all combination of options are available. Other specifications may be available upon request.

Specifications subject to change without notice.

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Parameter		LVDS						Unit	Test Condition
		3.3V		2.5V		1.8V			
		Min.	Max.	Min.	Max.	Min.	Max.		
Supply Voltage Variation (V_{DD})		V_{DD} – 10%	V_{DD} + 10%	V_{DD} – 5%	V_{DD} + 5%	V_{DD} – 5%	V_{DD} + 5%	V	
Frequency Range		13.5	220	13.5	220	13.5	220	MHz	
Standard Frequency		100, 125, 156.25						MHz	Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.
Power Current Consumption			35		30		20	mA	
Output Level	Differential Output (V_{OD}, OUT-OUTN)	0.24	0.45	0.24	0.45	0.24	0.45	V	
	Output High		1.6		1.6		1.6	V	
	Output Low	0.9		0.9		0.9		V	
Transition Time	Rise Time		0.3		0.3		0.5	nSec	Transition times are measured between 20% and 80%
	Fall Time		0.3		0.3		0.5	nSec	
Duty Cycle		45	55	45	55	45	55	%	
Startup Time			5		5		10	mSec	
Tri-State	Enable	0.7 x V_{DD}		0.7 x V_{DD}		0.7 x V_{DD}		V	
	Disable		0.3 x V_{DD}		0.3 x V_{DD}		0.3 x V_{DD}	V	
Stand by Current			10		10		10	µA	
Output Loading		100Ω (Between OUT & OUTN)						Ω	
RMS Phase Jitter Integrated 12 kHz~20 MHz @ 3.3V			0.3		0.3		0.3	pSec	
Aging (@ 25°C, First Year)			±3		±3		±3	ppm	
Storage Temp. Range		-55	125	-55	125	-55	125	°C	
Phase Noise		Typ.	Max.	Typ.	Max.	Typ.	Max.		
At V_{DD}=3.3V, fout=156.25MHz	10kHz offset	-145		-145		-142		dBc/Hz	
	100kHz offset	-153		-153		-150		dBc/Hz	
	1MHz offset	-155		-155		-153		dBc/Hz	

Parameter		HCSL						Unit	Test Condition
		3.3V		2.5V		1.8V			
		Min.	Max.	Min.	Max.	Min.	Max.		
Supply Voltage Variation (V_{DD})		V_{DD} – 10%	V_{DD} + 10%	V_{DD} – 5%	V_{DD} + 5%	V_{DD} – 5%	V_{DD} + 5%	V	
Frequency Range		100	135	100	135	100	135	MHz	
Standard Frequency		100, 125, 156.25						MHz	Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.
Power Current Consumption			42		42		30	mA	
Output Level	Output High	0.6	0.9	0.6	0.9	0.55	1.0	V	
	Output Low	-0.15	0.15	-0.15	0.15	-0.15	0.15	V	
Transition Time	Rise Time		0.6		0.6		0.6	nSec	Transition times are measured between 20% and 80%
	Fall Time		0.6		0.6		0.6	nSec	
Duty Cycle		45	55	45	55	45	55	%	
Startup Time			10		10		10	mSec	
Tri-State	Enable	0.7 x V_{DD}		0.7 x V_{DD}		0.7 x V_{DD}		V	
	Disable		0.3 x V_{DD}		0.3 x V_{DD}		0.3 x V_{DD}	V	
Stand by Current			10		10		10	µA	
Output Loading		50 to GND						Ω	
RMS Phase Jitter Integrated 12 kHz~20 MHz @ 3.3V			0.3		0.3		0.3	pSec	
Aging (@ 25°C, First Year)			±3		±3		±3	ppm	
Storage Temp. Range		-55	125	-55	125	-55	125	°C	
Phase Noise		Typ.	Max.	Typ.	Max.	Typ.	Max.		
At V_{DD}=3.3V, fout=156.25MHz	10kHz offset	-145		-145		-142		dBc/Hz	
	100kHz offset	-153		-153		-150		dBc/Hz	
	1MHz offset	-155		-155		-153		dBc/Hz	

FREQ. STABILITY vs. TEMP. RANGE

Temp.(°C) \ ppm	±25	±50
-20 ~ +70	○	○
-40 ~ +85	○	○
-40 ~ +105	X	○
-40 ~ +125	X	△

○: Available △:Conditional X: Not Available
Inclusive of calibration @ 25°C ,operating temperature rrange,input Voltage variation,load variation,aging (1st year),shock,and vibration

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