TPIC6B596 Power Logic 8-Bit Shift Register

1 Features

- Low $r_{DS(on)}$: 5Ω
- Avalanche energy: 30mJ
- Eight power DMOS-transistor outputs of 150-mA continuous current
- 500mA typical current-limiting capability
- Output clamp voltage: 50V
- Enhanced cascading for multiple stages
- All registers cleared with single input
- Low power consumption

2 Application

- Instrumentation Clusters
- Tell-Tale Lamps
- LED Illumination and Controls
- Automotive Relay or Solenoids Drivers

3 Description

The TPIC6B596 is a monolithic, high-voltage, medium-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium- current or high-voltage loads.

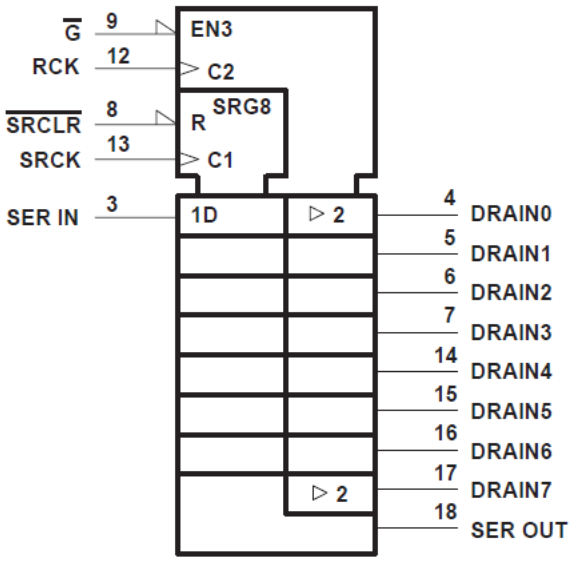
This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift- register clear ($\overline{SRCLR}$) is high. Write data and read data are valid only when RCK is low. When $\overline{SRCLR}$ is low, all registers in the device are cleared. When output enable ($\overline{G}$) is held high, all data in the output buffers is held low and all drain outputs are off. When $\overline{G}$ is held low, data from the storage register is transparent to the output buffers. When data in the output buffers is low, the DMOS- transistor outputs are off. When data is high, the DMOS-transistor outputs have sink-current capability. The serial output (SER OUT) is clocked out of the device on the falling edge of SRCK to provide additional hold time for cascaded applications. This will provide improved performance for applications where clock signals may be skewed, devices are not located near one another, or the system must tolerate electromagnetic interference.

Outputs are low-side, open-drain DMOS transistors with output ratings of 50V and 150mA continuous sink- current capability. Each output provides a 500mA typical current limit at T_C = 25°C. The current limit decreases as the junction temperature increases for additional device protection.

The TPIC6B596 is characterized for operation over the operating case temperature range of −40°C to 125°C.

Table 3-1. Device Information

PART MUMBER	PACKAGE	BODY SIZE(NOM)
TPIC6A595	PDIP(20)	25.4mm × 6.35mm
	SOIC(20)	12.80mm × 7.50mm



A. † This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Logic Symbol

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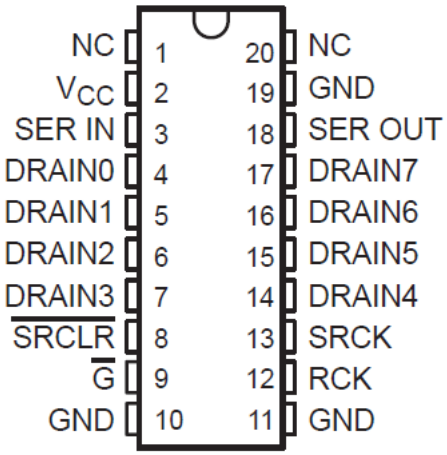
4 Pin Configuration and Functions



A. NC - No internal connection

Figure 4-1. DW or N Package (Top View)

Pin Function

PIN		I/O	DESCRIPTION
Name	NO.		
DRAIN0	4	O	Open-drain output
DRAIN1	5		
DRAIN2	6		
DRAIN3	7		
DRAIN4	14		
DRAIN5	15		
DRAIN6	16		
DRAIN7	17		
$\overline{G}$	9	I	Output enable, active-low
GND	10, 11, 19	-	Power ground
NC	1, 20	-	No internal connection
RCK	12	I	Register clock
SERIN	3	I	Serial data input
SEROUT	18	O	Serial data output
SRCK	15	I	Shift register clock
$\overline{SRCLR}$	3	I	Shift register clear, active-low
VCC	2	I	Power supply

5 Specifications

5.1 Absolute Maximum Ratings

over recommended operating case temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Logic supply voltage(2)			7	V
V_I	Logic input voltage range		-0.3	7	V
V_{DS}	Power DMOS drain-to-source voltage(3)			50	V
	Continuous source-to-drain diode anode current			500	mA
	Pulsed source-to-drain diode anode current(4)			1	A
I_D	Pulsed drain current, each output, all outputs on(4)	T_C = 25°C		500	mA
I_D	Continuous drain current, each output, all outputs on	T_C = 25°C		150	mA
I_{DM}	Peak drain current single output(4)	T_C = 25°C		500	mA
E_{AS}	Single-pulse avalanche energy (see Figure 6-4)			30	mJ
I_{AS}	Avalanche current(5)			500	mA
	Continuous total dissipation		See Section 5.2		
T_J	Operating virtual junction temperature range		-40	150	℃
T_C	Operating case temperature range		-40	125	℃
	Storage temperature range		-65	150	℃
	Lead temperature 1,6mm (1/16 inch) from case for 10 seconds			260	℃

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Each power DMOS source is internally connected to GND.
(4) Pulse duration ≤ 100 µs and duty cycle ≤ 2%.
(5) DRAIN supply voltage = 15V, starting junction temperature (T_{JS}) = 25°C, L = 200mH, I_{AS} = 0.5A (see Figure 6-4).

5.2 Dissipation Rating Table

PACKAGE	T_C ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
DW	1389mW	11.1mW/°C	278mW
N	1050mW	10. mW/°C	263mW

5.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Logic supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	0.85 V_{CC}		V
V_{IL}	Low-level input voltage		0.15 V_{CC}	V
	Pulsed drain output current, T_C = 25°C, V_{CC} = 5V(1) (2)	−500	500	mA
t_{su}	Setup time, SER IN high before SRCK (see Figure 6-2)	15		ns
t_h	Hold time, SER IN high after SRCK (see Figure 6-2)	15		ns
t_w	Pulse duration (see Figure 6-2)	40		ns
T_C	Operating case temperature	−40	125	°C

(1) Pulse duration ≤ 100µs and duty cycle ≤ 2%.
(2) Technique should limit $T_J - T_C$ to 10°C maximum.

5.4 Electrical Characteristics

V_{CC} = 5V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 1mA			50			V
V_{SD}	Source-to-drain diode forward voltage	I_F = 100mA				0.85	1	V
V_{OH}	High-level output voltage, SER OUT	I_{OH} = −20µA	V_{CC} = 4.5V		4.4	4.49		V
		I_{OH} = −4mA,	V_{CC} = 4.5V		4	4.2		
V_{OL}	Low-level output voltage, SER OUT	I_{OL} = 20µA,	V_{CC} = 4.5V			0.005	0.1	V
		I_{OL} = 4mA,	V_{CC} = 4.5V			0.3	0.5	
I_{IH}	High-level input current	V_{CC} = 5.5V,	$V_I = V_{CC}$				1	µA
I_{IL}	Low-level input current	V_{CC} = 5.5V,	V_I = 0				−1	µA
I_{CC}	Logic supply current	V_{CC} = 5.5V		All outputs off		20	100	µA
				All outputs on		150	300	
$I_{CC(FRQ)}$	Logic supply current at frequency	f_{SRCK} = 5MHz, All outputs off,		C_L = 30pF, See Figure 6-2 and Figure 5-2		0.4	5	mA
I_N	Nominal current	$V_{DS(on)}$ = 0.5V, $I_N = I_D$, T_C = 85°C		See(1) (2) (3)		90		mA
I_{DSX}	Off-state drain current	V_{DS} = 40V,	V_{CC} = 5.5V			0.1	5	µA
		V_{DS} = 40V,	V_{CC} = 5.5V,	T_C = 125°C		0.15	8	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 100mA,	V_{CC} = 4.5V	See Figure 5-3 and Figure 5-4 (1) (2)		4.2	5.7	Ω
		I_D = 100mA V_{CC} = 4.5V	T_C = 125°C,			6.8	9.5	
		I_D = 350mA,	V_{CC} = 4.5V			5.5	8	

(1) Technique should limit $T_J - T_C$ to 10°C maximum.
(2) These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
(3) Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5V at T_C = 85°C.

5.5 Switching Characteristics

V_{CC} = 5V, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from G	C_L = 30pF,	I_D = 100mA,		150		ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{G}$				90		ns
t_r	Rise time, drain output	See Figure 6-1, Figure 6-2 and Figure 5-5			200		ns
t_f	Fall time, drain output				200		ns
t_{pd}	Propagation delay time, SRCK↓ to SEROUT	C_L = 30pF, See Figure 6-2	I_D = 100mA,		15		ns
$f_{(SRCK)}$	Serial clock frequency	C_L = 30pF, See(3)	I_D = 100mA,			10	MHz
t_a	Reverse-recovery-current rise time	I_F = 100mA,	di/dt = 20A/µs,		100		ns
t_{rr}	Reverse-recovery time	See Figure 6-3 (1) (2)			300		

(1) Technique should limit $T_J - T_C$ to 10°C maximum.
(2) These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
(3) This is the maximum serial clock frequency assuming cascaded operation where serial data is passed from one stage to a second stage. The clock period allows for SRCK → SEROUT propagation delay and setup time plus some timing margin.

5.6 Thermal Resistance

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	DW package	All 8 outputs with equal power		90	°C/W
		N package			95	

5.7 Typical Characteristics

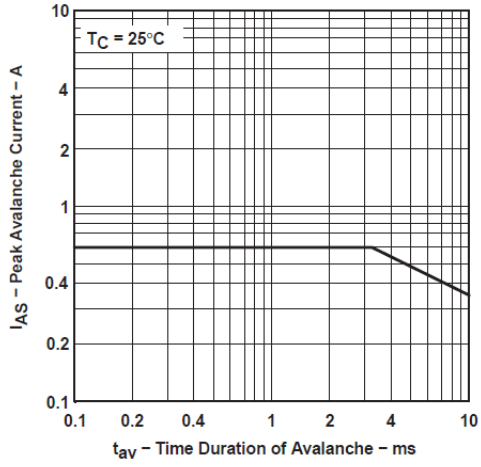


Figure 5-1. Peak Avalanche Current vs Time Duration of Avalanche

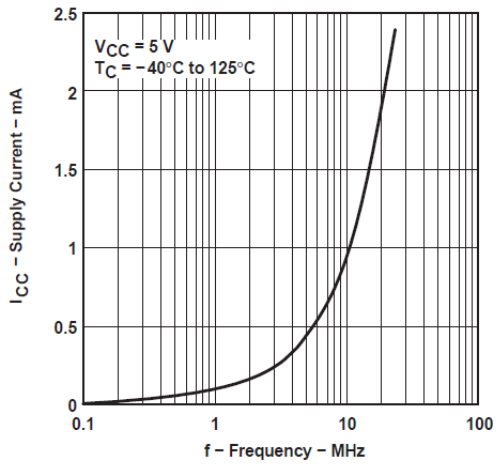


Figure 5-2. Supply Current vs Frequency

5.7 Typical Characteristics (continued)

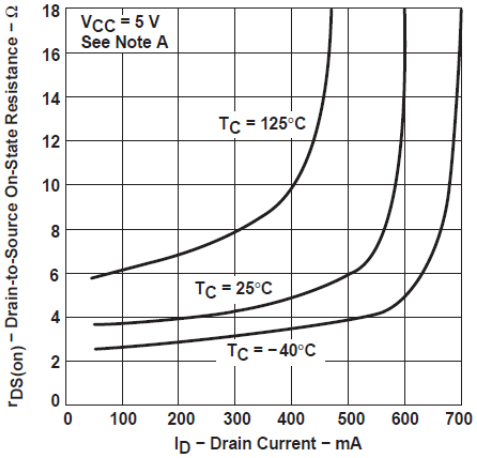


Figure 5-3. Drain-to-Source On-State Resistance vs Drain Current

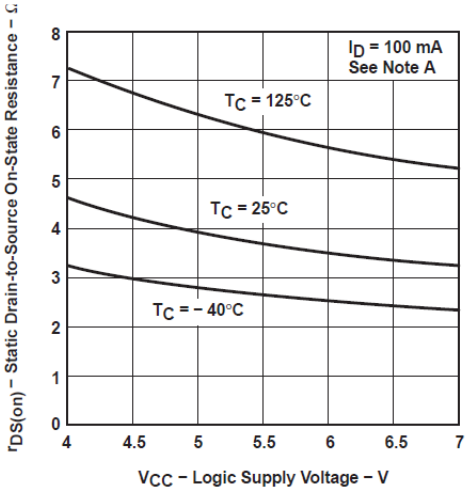
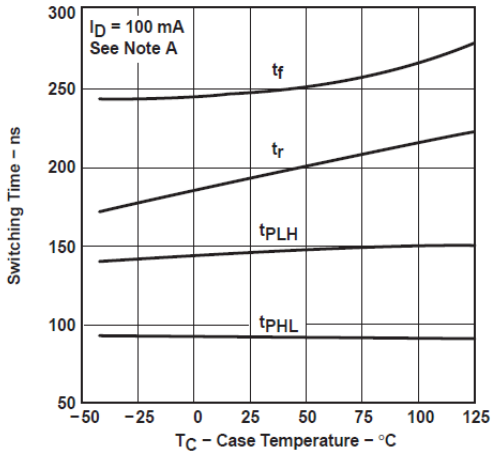


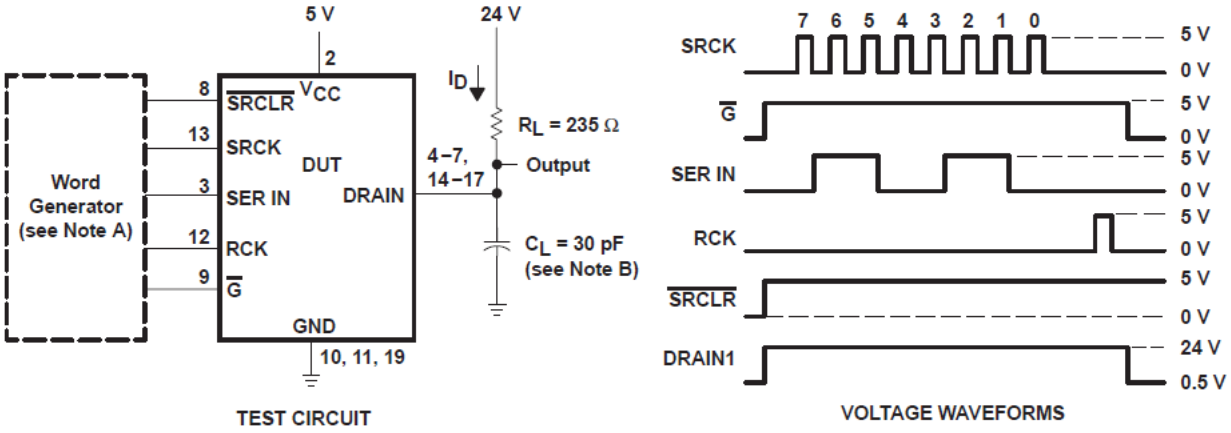
Figure 5-4. Static Drain-to-Source On-State Resistance vs Logic Supply Voltage



Technique should limit $T_J - T_C$ to 10°C maximum.

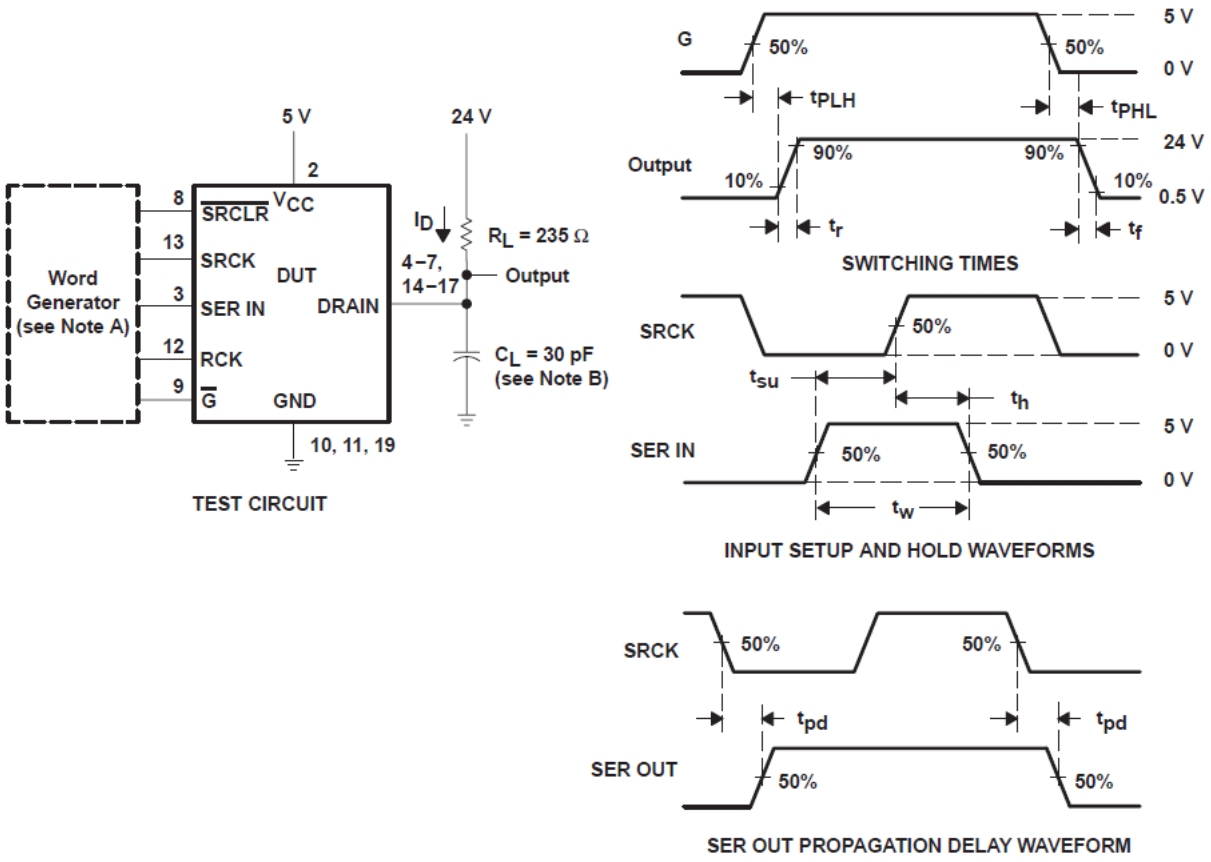
Figure 5-5. Switching Time vs Case Temperature

6 Parameter Measurement Information



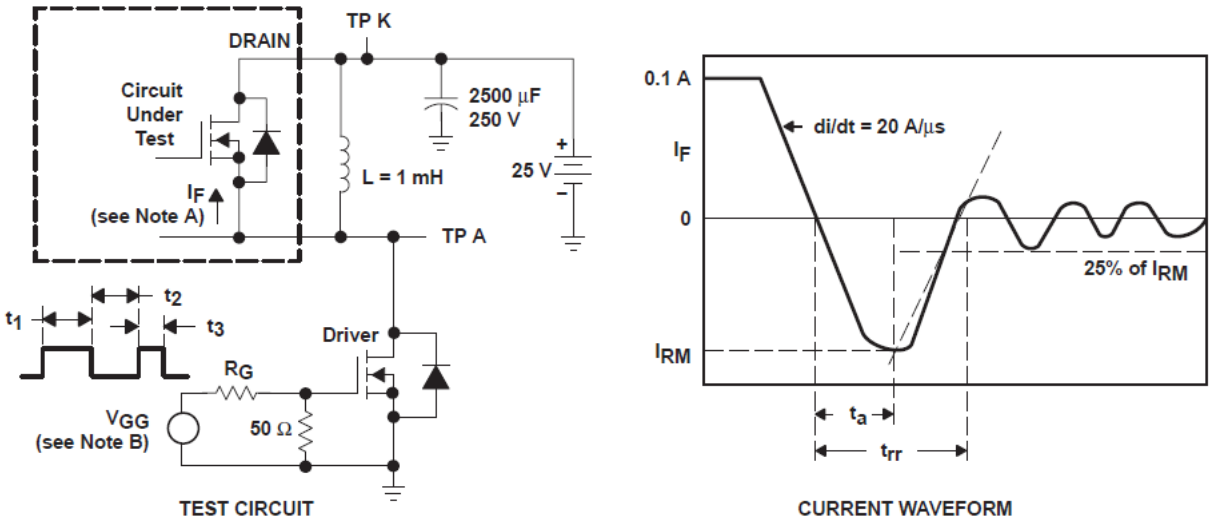
A. The word generator has the following characteristics: $t_r \le 10ns$, $t_f \le 10ns$, $t_w = 300ns$, pulsed repetition rate (PRR) = 5kHz, $Z_O = 50\Omega$.
B. C_L includes probe and jig capacitance.
C. Write data and read data are valid only when RCK is low

Figure 6-1. Resistive-Load Test Circuit and Voltage Waveforms



A. The word generator has the following characteristics: $t_r \le 10ns$, $t_f \le 10ns$, $t_w = 300ns$, pulsed repetition rate (PRR) = 5kHz, $Z_O = 50\Omega$.
B. C_L includes probe and jig capacitance

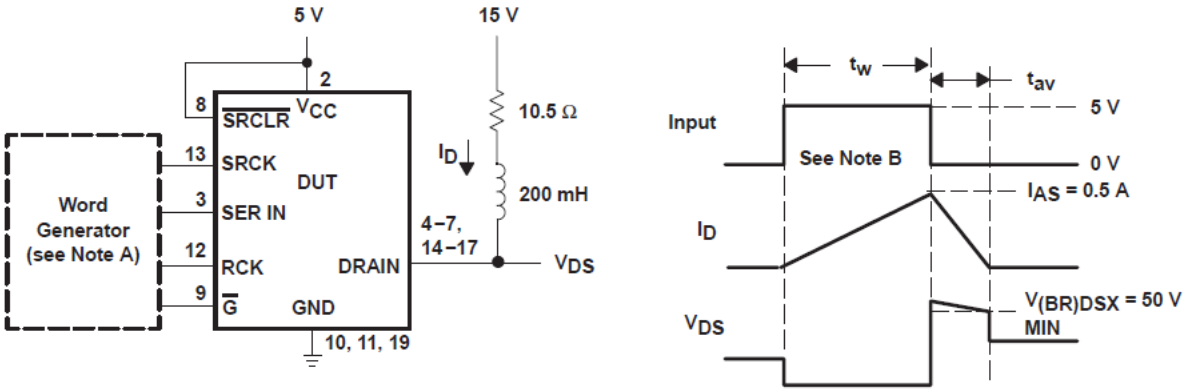
Figure 6-2. Test Circuit, Switching Times, and Voltage Waveforms



A. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

B. The V_{GG} amplitude and R_G are adjusted for di/dt = 20A/µs. A V_{GG} double-pulse train is used to set I_F = 0.1A, where t_1 = 10µs, t_2 = 7µs, and t_3 = 3µs.

Figure 6-3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-to-Drain Diode



A. The word generator has the following characteristics: $t_r \leq 10ns$, $t_f \leq 10ns$, $Z_O = 50\Omega$.

B. Input pulse duration, t_w, is increased until peak current I_{AS} = 0.5A.
Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2$ = 30mJ.

Figure 6-4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

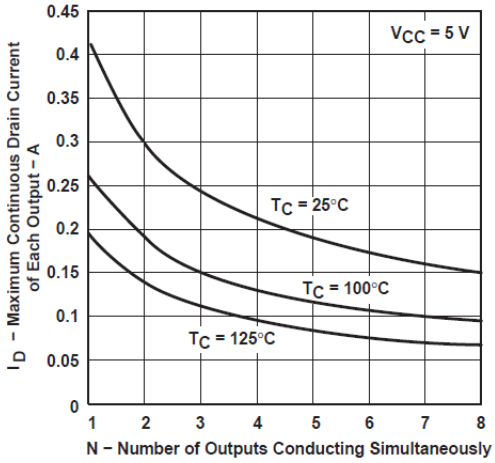


Figure 6-5. Maximum Continuous Drain Current of Each Output vs Number of Outputs Conducting Simultaneously

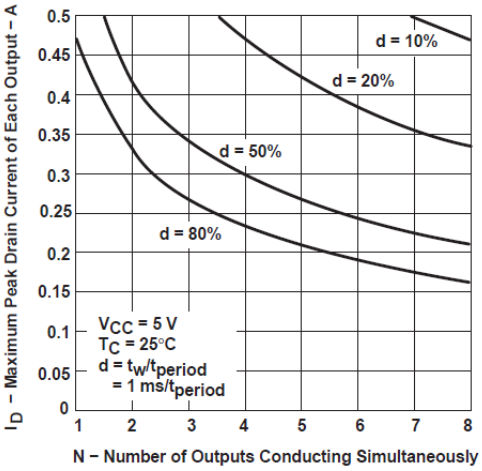


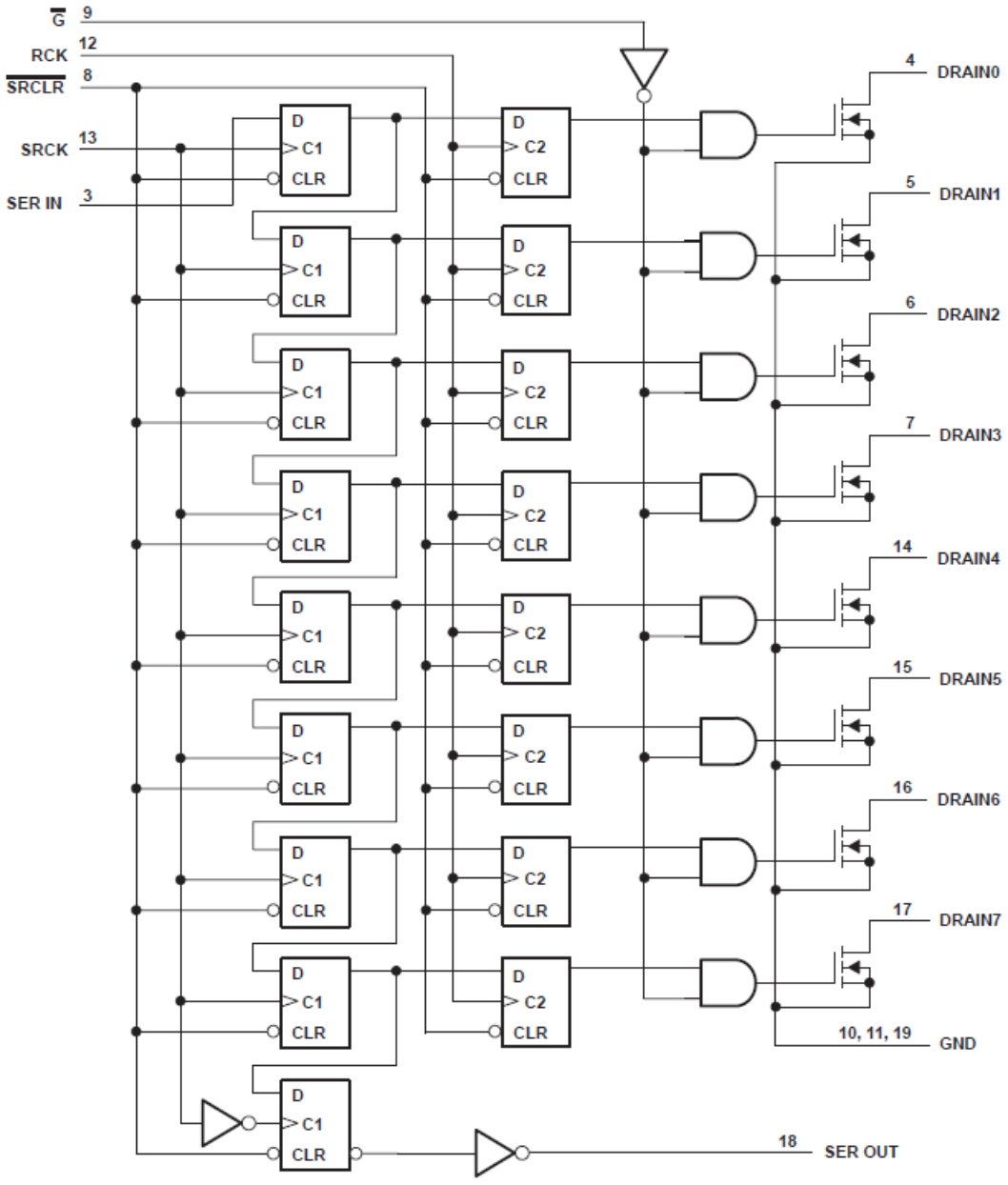
Figure 6-6. Maximum Peak Drain Current of Each Output vs Number of Outputs Conducting Simultaneously

7 Detailed Description

7.1 Overview

The TPIC6B596 device is a monolithic, high-voltage, medium-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection, so it can also drive relays, solenoids, and other medium-current or high-voltage loads.

7.2 Functional Block Diagram



Functional Block Diagram

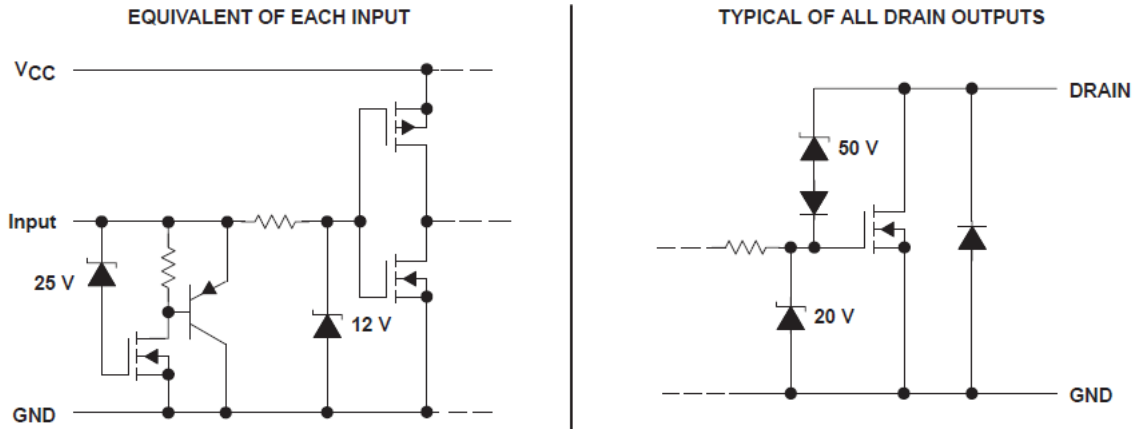


Figure 7-1. Functional Block Diagram (continued)

7.3 Reference

7.3.1 Reference

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift register clock (SRCK) and the register clock (RCK), respectively. Write data and read data are valid only when RCK is low. The storage register transfers data to the output buffer when shift register clear ($\overline{\text{SRCLR}}$) is high.

7.3.2 Clear Register

A logical low on ($\overline{\text{SRCLR}}$) clears all registers in the device. TI suggests clearing the device during power up or initialization.

7.3.3 Output Control

Holding the output enable ($\overline{\text{G}}$) high holds all data in the output buffers low, and all drain outputs are off. Holding ($\overline{\text{G}}$) low makes data from the storage register transparent to the output buffers. When data in the output buffers is low, the DMOS transistor outputs are OFF. When data is high, the DMOS transistor outputs have sink-current capability. This pin can also be used for global PWM dimming.

7.3.4 Cascaded Application

The serial output (SER OUT) allows for cascading of the data from the shift register to additional devices. The serial output (SER OUT) is clocked out of the device on the falling edge of SRCK to provide additional hold time for cascaded applications. This will provide improved performance for applications where clock signals may be skewed, devices are not located near one another, or the system must tolerate electromagnetic interference. Connect the device (SER OUT) pin to the next device (SER IN) for daisy Chain.

7.3.5 Current Limit Function

Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and 150-mA continuous sink current capability. Each output provides a 500-mA typical current limit at TC = 25°C. The current limit decreases as the junction temperature increases for additional device protection.

8 Device Functional Modes

8.1 Operating with V_{cc} < 4.5V

This device works normally during 4.5V ≤ V_{cc} ≤ 5.5V, when operation voltage is lower than 4.5V, correct behavior of the device, including communication interface and current capability, is not assured.

8.2 Operating with 5.5V < V_{cc} ≤ 7V

The device works normally in this voltage range, but reliability issues can occur if the device works for a long time in this voltage range.

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2005) to Revision B (March 2024)	Page
• Updated Applications section	1

Changes from Revision * (March 2000) to Revision A (May 2005)	Page
• Changed $\overline{\text{SRCLR}}$ timing diagram in Figure 6-1	8

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPIC6B596DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 125	TPIC6B596	
TPIC6B596DWG4	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI		TPIC6B596	
TPIC6B596DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC6B596	Samples
TPIC6B596DWRG4	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI		TPIC6B596	
TPIC6B596N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TPIC6B596N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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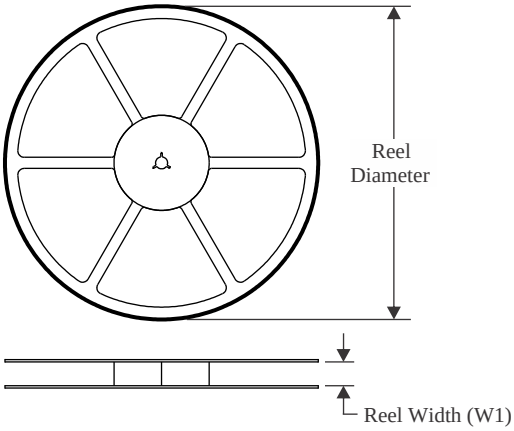
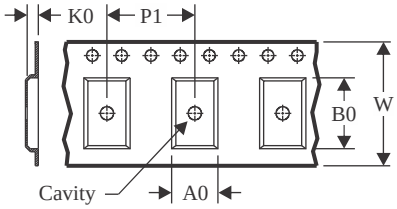
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

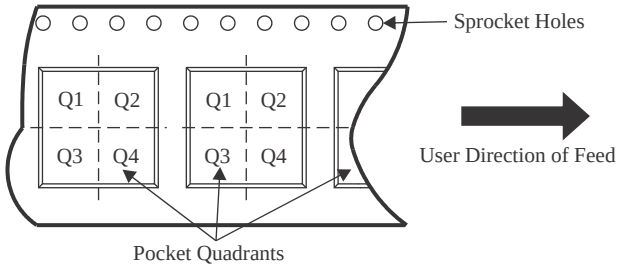


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

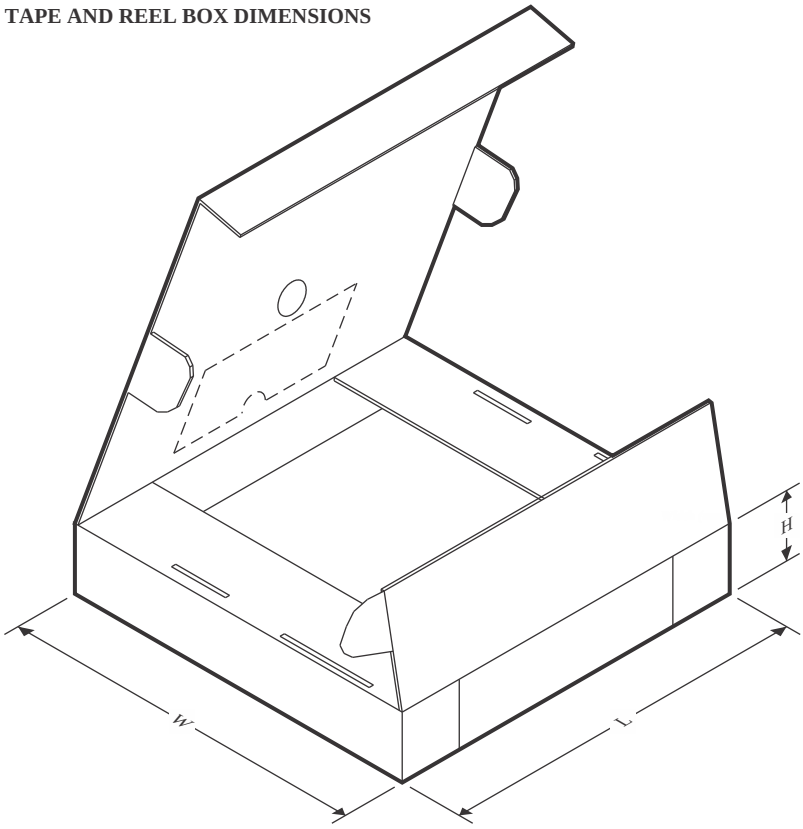
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPIC6B596DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TPIC6B596DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

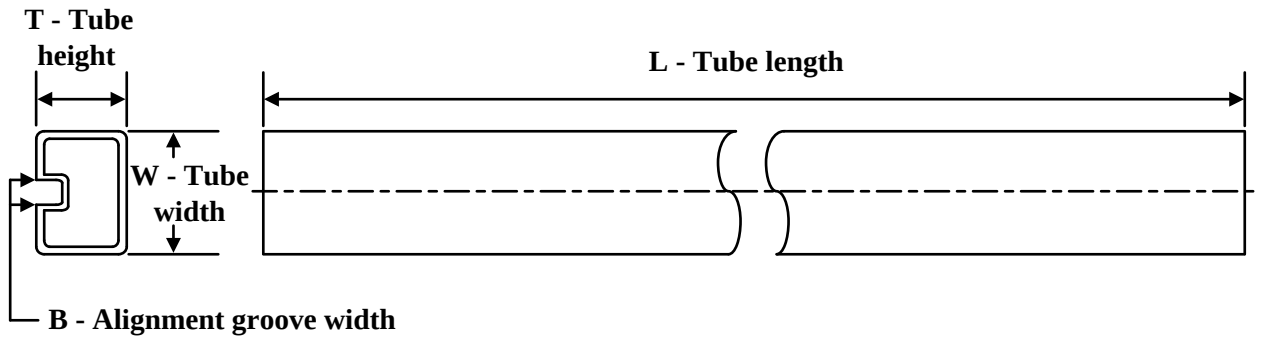
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPIC6B596DWR	SOIC	DW	20	2000	350.0	350.0	43.0
TPIC6B596DWR	SOIC	DW	20	2000	350.0	350.0	43.0

TUBE



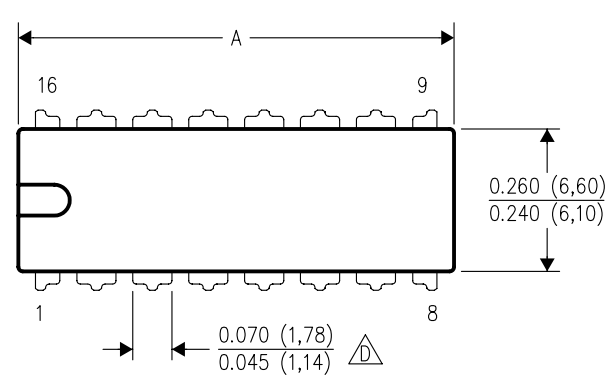
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPIC6B596N	N	PDIP	20	20	506	13.97	11230	4.32

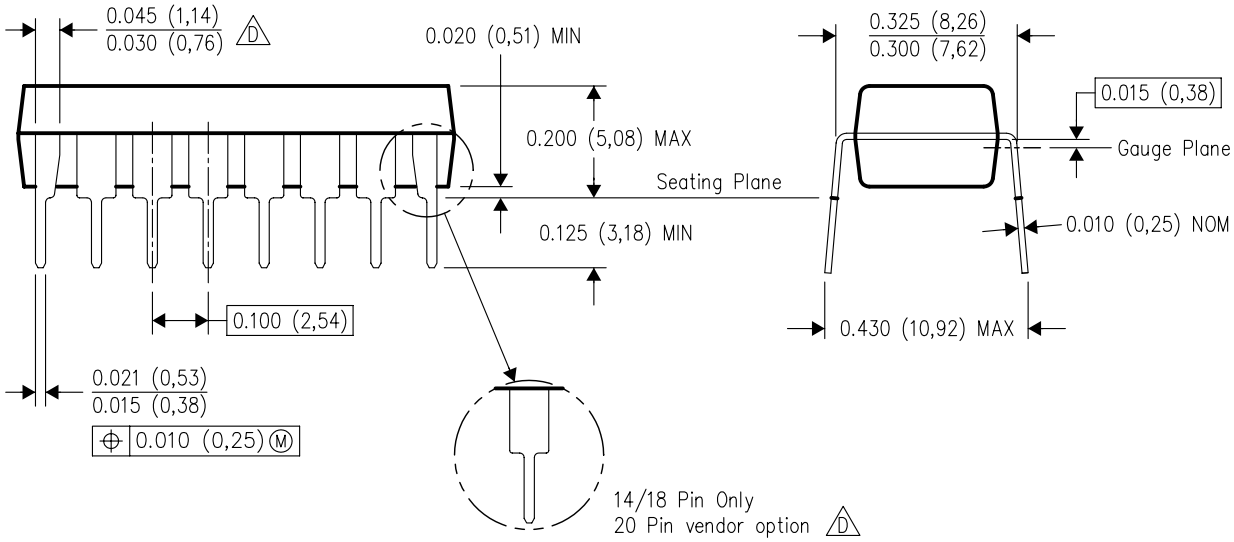
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

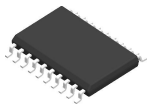


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

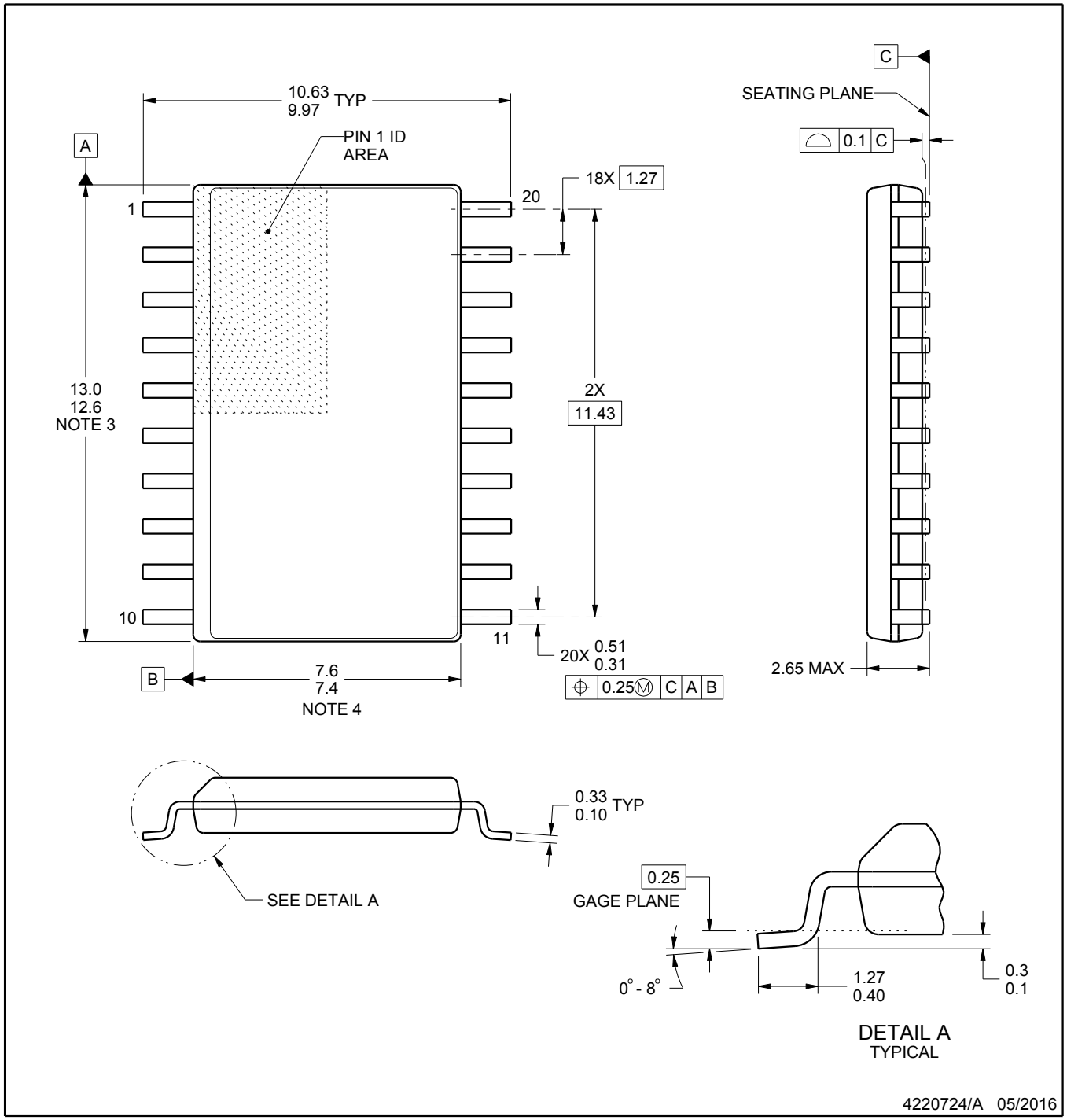


PACKAGE OUTLINE

DW0020A

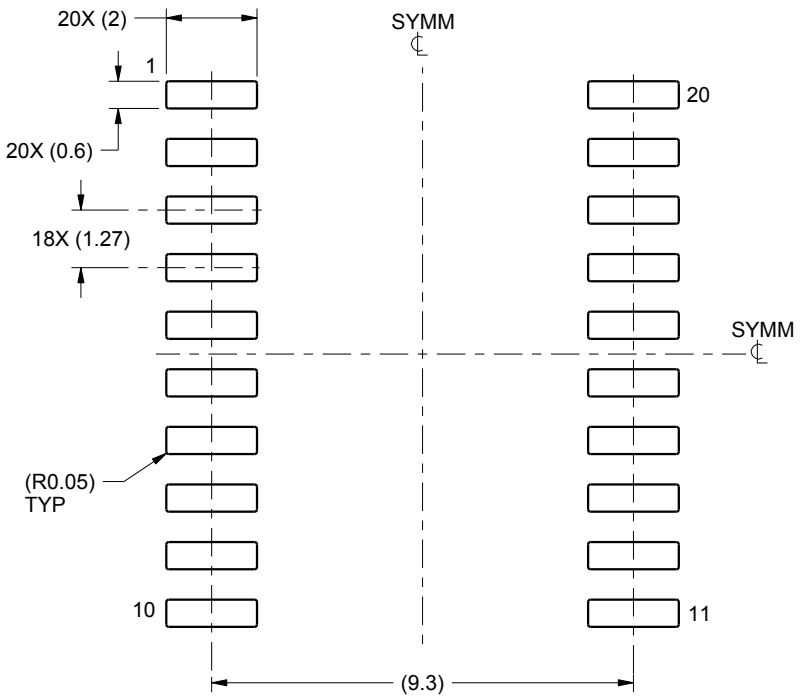
SOIC - 2.65 mm max height

SOIC

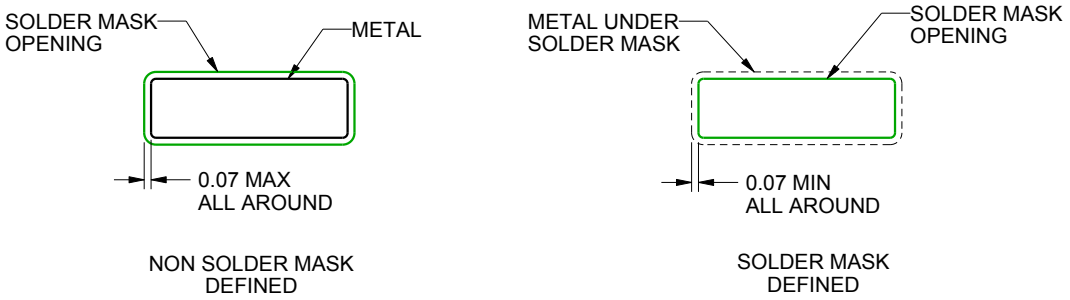


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

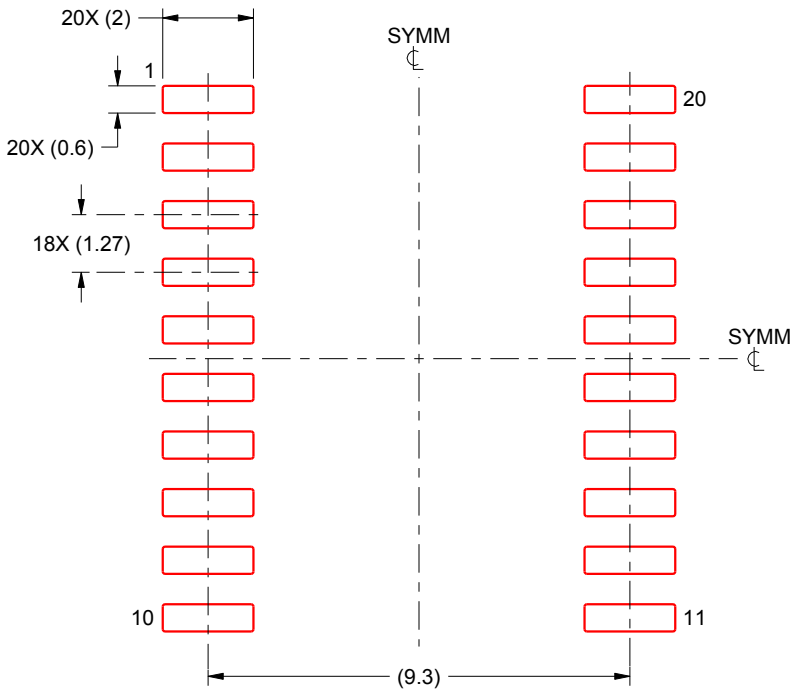


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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