L6494

Datasheet

High voltage high and low-side 2 A gate driver

SO-14

STDRIVE

Product status link

L6494

Product label

SUSTAINABLE TECHNOLOGY

Features

- Transient withstand voltage 600 V
- dV/dt immunity ± 50 V/ns in full temperature range
- Driver current capability:
  - 2 A source typ. at 25 °C
  - 2.5 A sink typ. at 25 °C
- Short propagation delay: 85 ns
- Switching times 25 ns rise/fall with 1 nF load
- Integrated bootstrap diode
- Single input and shutdown pin
- Adjustable deadtime
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- UVLO on both high-side and low-side sections
- Compact and simplified layout
- Bill of material reduction
- Flexible, easy and fast design

Applications

- Motor driver for home appliances, factory automation, industrial drives, fans
- HID ballasts
- Induction heating
- Welding
- UPS
- Power supply units
- DC-DC converters

Description

The L6494 is a high voltage device manufactured with the BCD6 “OFF-LINE” technology. It is a single-chip half-bridge gate driver for N-channel power MOSFETs or IGBTs.

The high-side (floating) section is designed to stand a voltage rail up to 500 V, with 600 Vtransient withstand voltage. The logic inputs are CMOS/TTL compatible down to 3.3 V for easy interfacing microcontroller or DSP.

The device is a single input gate driver with programmable deadtime, and also features an active-low shutdown pin.

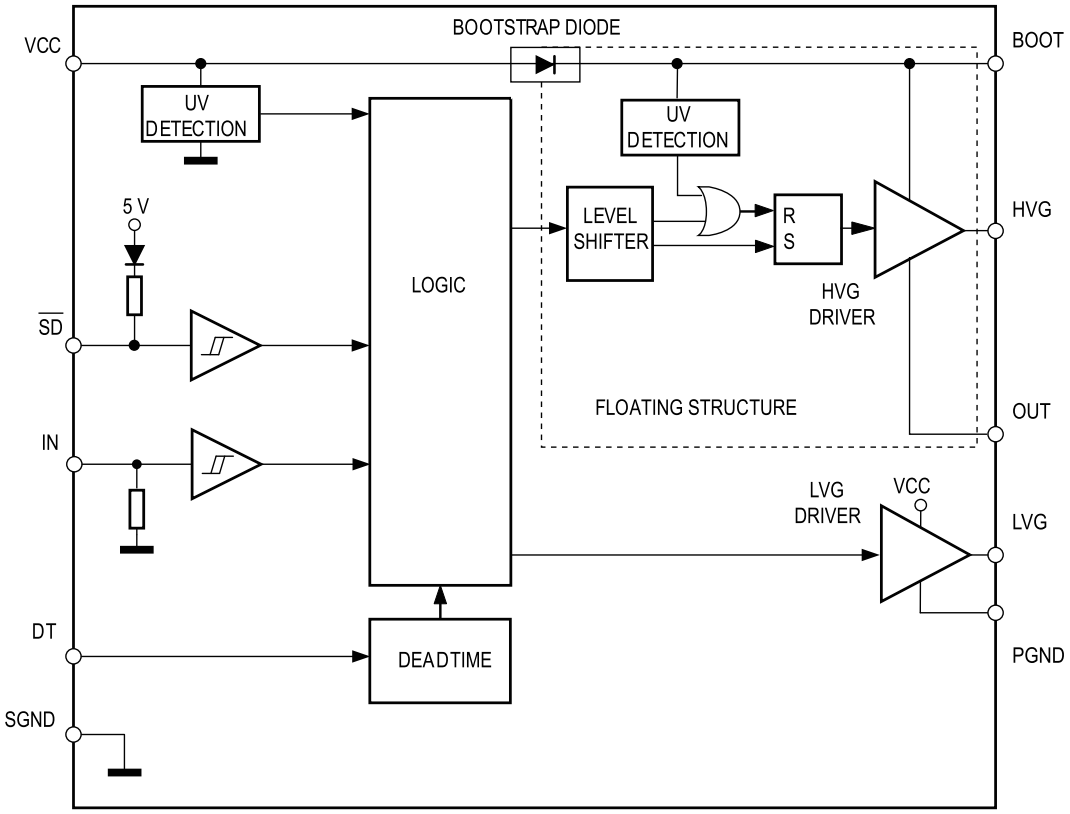
Both device outputs can sink 2.5 A and source 2 A, making the L6494 particularly suited for medium and high capacity power MOSFETs\IGBTs.

The independent UVLO protection circuits present on both the lower and upper driving sections prevent the power switches from being operated in low efficiency or dangerous conditions.

The integrated bootstrap diode as well as all of the integrated features of this driver make the application PCB design simpler and more compact, and help reducing the overall bill of material.

1 Block diagram

Figure 1. **Block diagram**



2 Pin description and connection diagram

Figure 2. **Pin connection SO-14 (top view)**

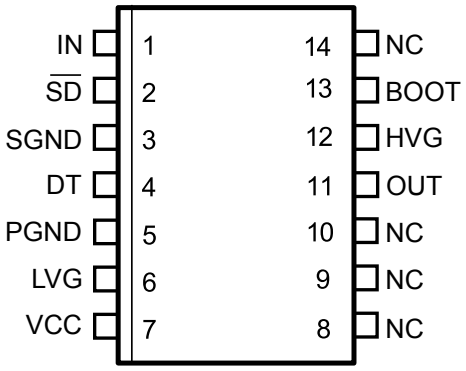


Table 1. **Pin description**

Pin number	Pin name	Type	Function
1	IN	I	Output drivers logic input (is in phase with HVG and in opposition of phase with LVG)
2	$\overline{SD}$	-	Shutdown logic input (active low)
3	SGND	P	Signal ground
4	DT	I	Deadtime setting
5	PGND	P	Power ground
6	LVG (1)	O	Low-side driver output
7	VCC	P	Low-side section supply voltage
11	OUT	P	High-side (floating) section common voltage
12	HVG (1)	O	High-side driver output
13	BOOT	P	High-side (bootstrapped) section supply voltage
8, 9, 10, 14	NC	-	Not connected

1. *The circuit guarantees less than 1 V on the LVG and HVG pins (at I_{sink} = 10 mA), with V_{CC} > 3 V. This allows omitting the "bleeder" resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low.*

3 Electrical data

3.1 Absolute maximum ratings

Absolute maximum ratings are those values beyond which damage to the device may occur. These are stress ratings only and functional operation of the device at these conditions is not implied. Operating outside maximum recommended conditions for extended periods of time may impact product reliability and result in device failures.

Table 2. Absolute maximum ratings

Each voltage referred to SGND unless otherwise specified.

Symbol	Parameter	Value		Unit
		Min.	Max.	
V_{CC}	Supply voltage	- 0.3	21	V
V_{PGND}	Low-side driver ground	V_{CC} - 21	V_{CC} + 0.3	V
V_{OUT}	Output voltage	V_{BOOT} - 21	V_{BOOT} + 0.3	V
V_{BOOT}	Boot DC voltage	-0.3	500	V
	Boot transient withstand voltage (T_{pulse} < 1 ms)	-	620	V
V_{hvg}	High-side gate output voltage	V_{OUT} - 0.3	V_{BOOT} + 0.3	V
V_{lvg}	Low-side gate output voltage	PGND - 0.3	V_{CC} + 0.3	V
V_i	Logic input voltage	-0.3	15	V
dV_{OUT}/dt	Allowed output slew rate	-	50	V/ns
P_{TOT}	Total power dissipation (T_{amb} = 25 °C)	-	1.0	W
T_J	Junction temperature	-	150	°C
T_{stg}	Storage temperature	-50	150	°C
ESD	Human body model	2		kV

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Package	Value	Unit
$R_{th\ (JA)}$	Thermal resistance junction to ambient	SO-14	120	°C/W

3.3 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Pin	Parameter	Test conditions	Min.	Max.	Unit
VCC	VCC	Supply voltage	-	10	20	V
V_{PS} (1)	SGND - PGND	Low-side driver ground	-	-5	+5	V
V_{BO} (2)	BOOT - OUT	Floating supply voltage	-	9.3	20	V
V_{OUT}	OUT	OUT DC voltage	-	-9 (3)	480	V
		OUT transient withstand voltage	T_{pulse} < 1 ms	-	600	V
f_{sw}	-	Maximum switching frequency	HVG, LVG load C_L = 1 nF	-	800	kHz
T_J	-	Junction temperature	-	-40	125	°C
T_{amb}	-	Ambient temperature (4).	-	-40	125	°C

1. *V_{PS} = V_{PGND} - SGND.*
2. *V_{BO} = V_{BOOT} - V_{OUT}.*
3. *LVG off. V_{CC} = 12.5 V. Logic is operational if V_{BOOT} > 5 V.*
4. *Maximum ambient temperature is actually limited by T_J*

4 Electrical characteristics

Table 5. Electrical characteristics

VCC = 15 V; PGND = SGND; T_J = + 25 °C

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Low-side section supply							
V_{CC_hys}	VCC vs. SGND	V_{CC} UV hysteresis		0.5	0.6	0.72	V
V_{CC_thON}		V_{CC} UV turn-ON threshold		8.7	9.3	9.8	V
V_{CC_thOFF}		V_{CC} UV turn-OFF threshold		8.2	8.7	9.2	V
I_{qccu}		Undervoltage quiescent supply current	VCC = $\overline{SD}$ = 7 V IN = DT = SGND	-	135	200	µA
I_{qcc}		Quiescent current	VCC = 15 V $\overline{SD}$ = 5 V; IN = DT = SGND	-	490	700	µA
Bootstrapped supply voltage section (1)							
V_{BO_hys}	BOOT vs. OUT	V_{BO} UV hysteresis		0.48	0.6	0.7	V
V_{BO_thON}		V_{BO} UV turn-ON threshold		8	8.6	9.1	V
V_{BO_thOFF}		V_{BO} UV turn-OFF threshold		7.5	8.0	8.5	V
I_{QBOU}		Undervoltage V_{BO} quiescent current	V_{BO} = $\overline{SD}$ = 7 V IN = SGND	-	20	30	µA
I_{QBO}		V_{BO} quiescent current	V_{BO} = 15 $\overline{SD}$ = IN = 5 V	-	90	120	µA
I_{LK}		High voltage leakage current	BOOT = HVG = OUT = 600 V	-	-	8	µA
$R_{DS(on)}$		Bootstrap driver on resistance (2)		-	175	-	Ω
Driving buffer section							
I_{so}	LVG, HVG	High/low-side source peak current	LVG/HVG high T_J = 25 °C	1.6	2.0	-	A
			Full temperature range (3)	1.25	-	-	A
I_{si}		High/low-side sink peak current	LVG/HVG low T_J = 25 °C	2.0	2.5	-	A
			Full temperature range (3)	1.55	-	-	A
Logic inputs							
V_{il}	IN, $\overline{SD}$, vs. SGND	Low level logic threshold		0.95	-	1.45	V
V_{ih}		High level logic threshold voltage		2	-	2.5	V
I_{INh}	IN vs. SGND	IN logic “1” input bias current	IN = 15 V	120	200	260	µA
I_{INl}		IN logic “0” input bias current	IN = 0 V	-	-	1	µA
R_{PD_IN}		IN pull-down resistor	IN = 15 V	58	75	125	kΩ
I_{SDh}	$\overline{SD}$ vs. SGND	$\overline{SD}$ logic “1” input bias current	$\overline{SD}$ = 15 V	-	-	1	µA
I_{SDl}		$\overline{SD}$ logic “0” input bias current	$\overline{SD}$ = 0 V	14	17	23	µA
R_{PU_SD}		$\overline{SD}$ pull-up resistor	$\overline{SD}$ = 0 V	58	75	125	kΩ

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Dynamic characteristics (see Figure 3 and Figure 4)							
t_{on}	$\overline{SD}$ vs. LVG/HVG	High/low-side driver turn-on propagation delay	V_{OUT} = 0 V; V_{BOOT} = V_{CC} C_L = 1 nF; V_i = 0 to 3.3 V	-	85	120	ns
t_{off}	$\overline{SD}$ vs. LVG/HVG; IN vs. LVG/HVG	High/low-side driver turn-off propagation delay		-	85	120	ns
MT	-	Delay matching, HS and LS turn on/off (4)	-	-	-	30	ns
t_r	LVG, HVG	Rise time	C_L = 1 nF	-	25	-	ns
t_f		Fall time	C_L = 1 nF	-	25	-	ns
DT	-	Deadtime setting range	R_{DT} = 0 Ω, C_L = 1 nF	0.34	0.44	0.54	µs
			R_{DT} = 100 kΩ, C_L = 1 nF C_{DT} = 100 nF	2.10	2.70	3.30	µs
			R_{DT} = 200 kΩ, C_L = 1 nF C_{DT} = 100 nF	4.00	5.00	6.00	µs
MDT	-	Matching deadtime (5)	R_{DT} = 0 Ω, C_L = 1 nF	-	-	85	ns
			R_{DT} = 100 kΩ, C_L = 1 nF C_{DT} = 100 nF	-	-	350	ns
			R_{DT} = 200 kΩ, C_L = 1 nF C_{DT} = 100 nF	-	-	700	ns

1. *V_{BO} = V_{BOOT} - V_{OUT}.*
2. *$R_{DS(on)}$ is tested in the following way:*
   $R_{DS(on)}$ = [(V_{CC} - V_{BOOT1}) - (V_{CC} - V_{BOOT2})] / [I_1(V_{CC}, V_{BOOT1}) - I_2(V_{CC}, V_{BOOT2})]
   where I_1 is BOOT pin current when V_{BOOT} = V_{BOOT1}, I_2 when V_{BOOT} = V_{BOOT2}.
3. *Characterized, not tested in production.*
4. *MT = max. (|$t_{on(LVG)}$ - $t_{off(LVG)}$|, |$t_{on(HVG)}$ - $t_{off(HVG)}$|, |$t_{off(LVG)}$ - $t_{on(HVG)}$|, |$t_{off(HVG)}$ - $t_{on(LVG)}$|).*
5. *MDT = | DT_{LH} - DT_{HL} | (see Figure 4).*

Figure 3. $\overline{SD}$ timings

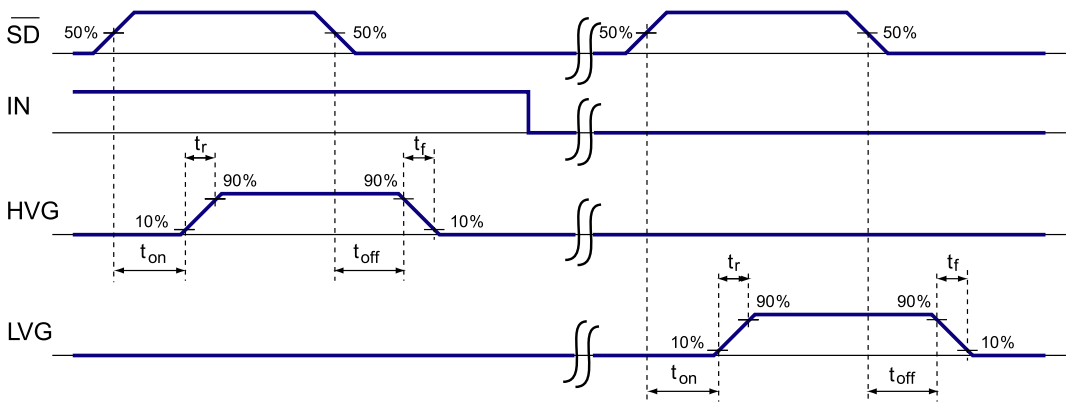


Figure 4. **IN timings and deadtime**

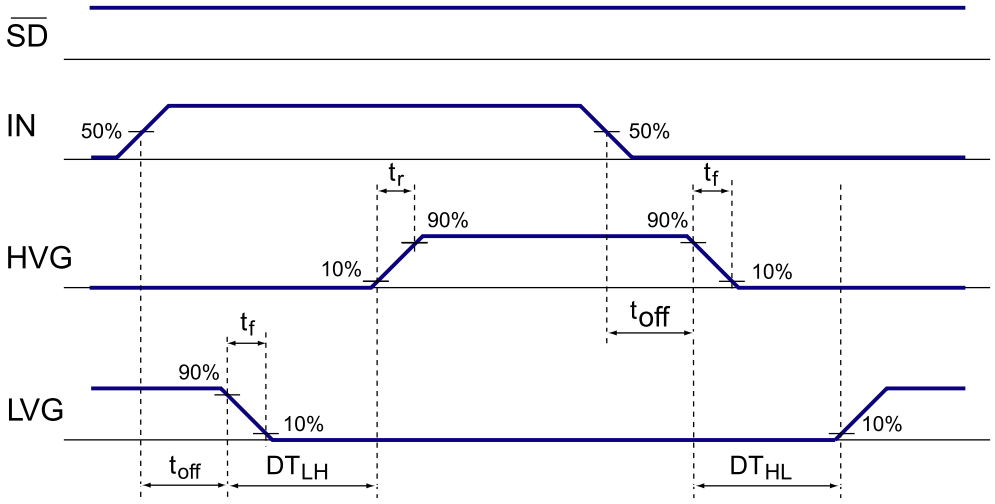
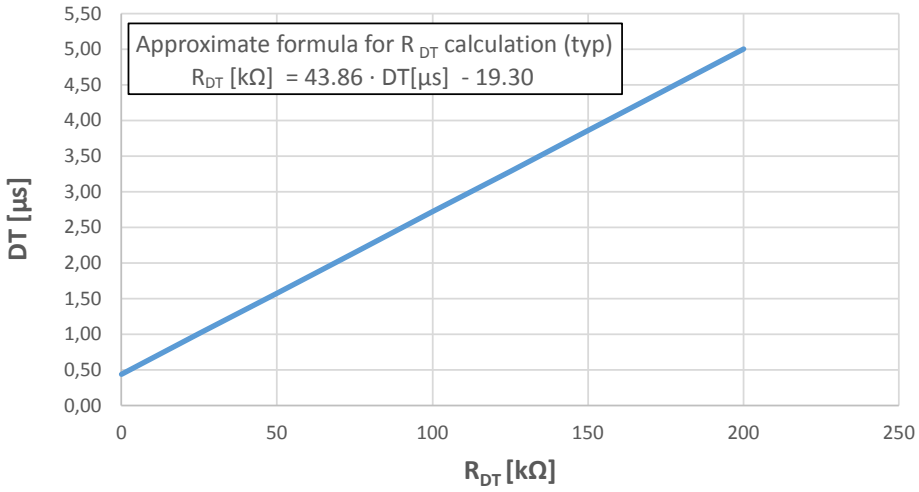


Figure 5. **Typical deadtime vs. DT resistor value**



5 Truth table

Table 6. **Truth table**

Input		Output	
$\overline{SD}$	IN	LVG	HVG
L	X (1)	L	L
H	L	H	L
H	H	L	H

1. *X: don't care.*

6 Typical application diagram

Figure 6. **Typical application diagram**

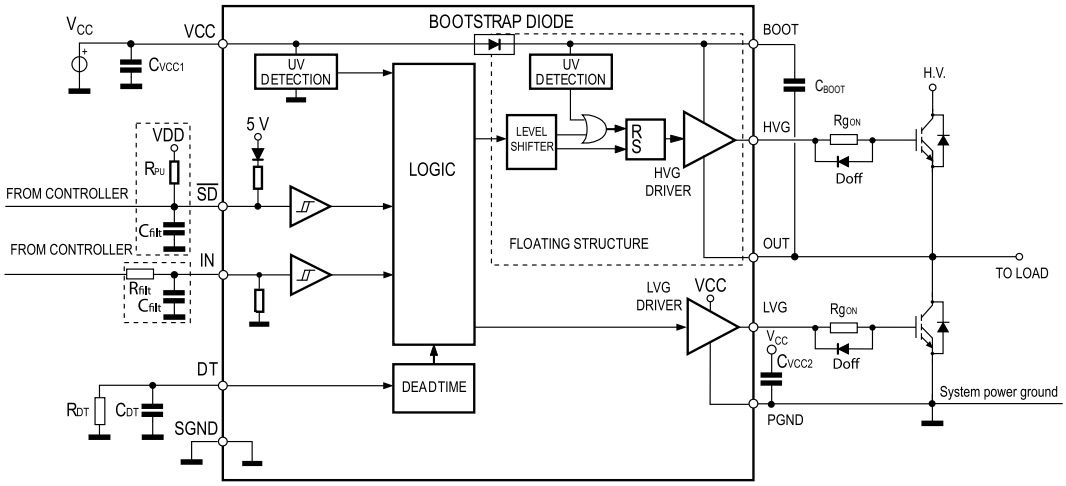
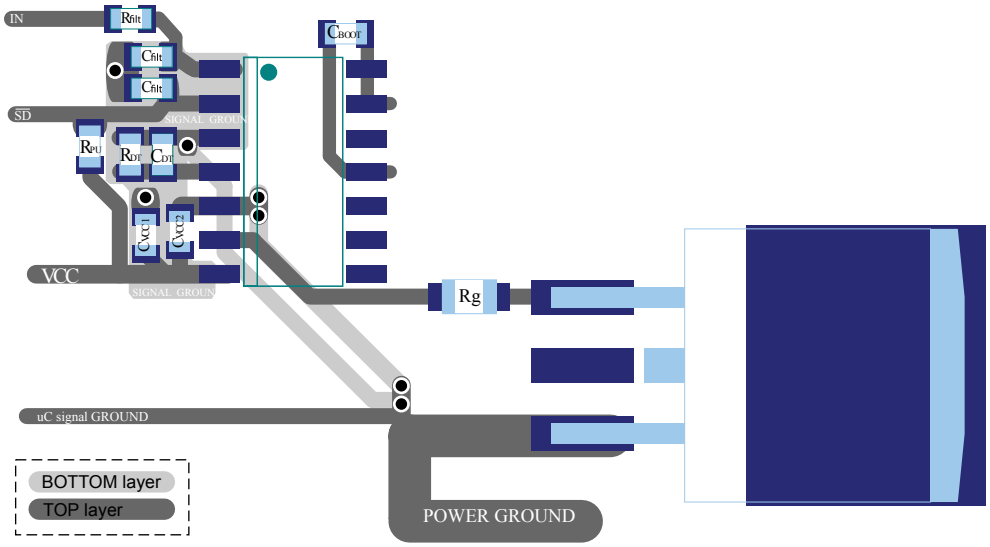


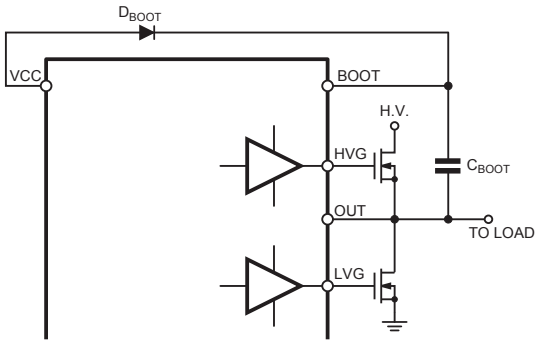
Figure 7. **Suggested PCB layout (SO-14)**



7 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is usually accomplished by a high voltage fast recovery diode (see Figure 8). In the L6494 an integrated structure replaces the external diode.

Figure 8. Bootstrap driver with external high voltage fast recovery



7.1 C_{BOOT} selection and charging

To choose the proper C_{BOOT} value the external MOS can be seen as an equivalent capacitor.

This capacitor C_{EXT} is related to the MOS total gate charge:

Equation 1

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}} \quad (1)$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss. It must be: $C_{BOOT} >> C_{EXT}$.

For example: if Q_{gate} is 30 nC and V_{gate} is 10 V, C_{EXT} is 3 nF. With C_{BOOT} = 100 nF the drop would be 300 mV.

If HVG must be supplied for a long period, the C_{BOOT} selection must take into account also the leakage and quiescent losses.

For example: HVG steady-state consumption is lower than 120 µA, therefore, if HVG t_{on} is 5 ms, C_{BOOT} must supply 0.6 µC to C_{EXT}. This charge on a 1 µF capacitor means a voltage drop of 0.6 V.

The internal bootstrap driver offers a big advantage: the external fast recovery diode can be avoided (it usually has very high leakage current). This structure can work only if V_{OUT} is close to SGND (or lower) and, in the meantime, the LVG is on. The charging time (t_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it Must be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS $R_{DS(on)}$ (typical value: 175 Ω). This drop can be neglected at low switching frequency, but it should be taken into account when operating at high switching frequency.

is useful to compute the drop on the bootstrap DMOS:

Equation 2

$$V_{drop} = I_{charge} \cdot R_{DS(on)} \rightarrow V_{drop} = \frac{Q_{gate}}{t_{charge}} \cdot R_{DS(on)} \quad (2)$$

where Q_{gate} is the gate charge of the external power MOS, $R_{DS(on)}$ is the ON-resistance of the bootstrap DMOS, and t_{charge} is the charging time of the bootstrap capacitor.

For example: using a power MOS with a total gate charge of 30 nC, the drop on the bootstrap DMOS is about 1 V, if the t_{charge} is 5 µs. In fact:

Equation 3

$$V_{drop} = \frac{30nC}{5\mu s} \cdot 175\Omega \sim 1V \quad (3)$$

V_{drop} should be taken into account when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 SO-14 package information

Figure 9. SO-14 package outline

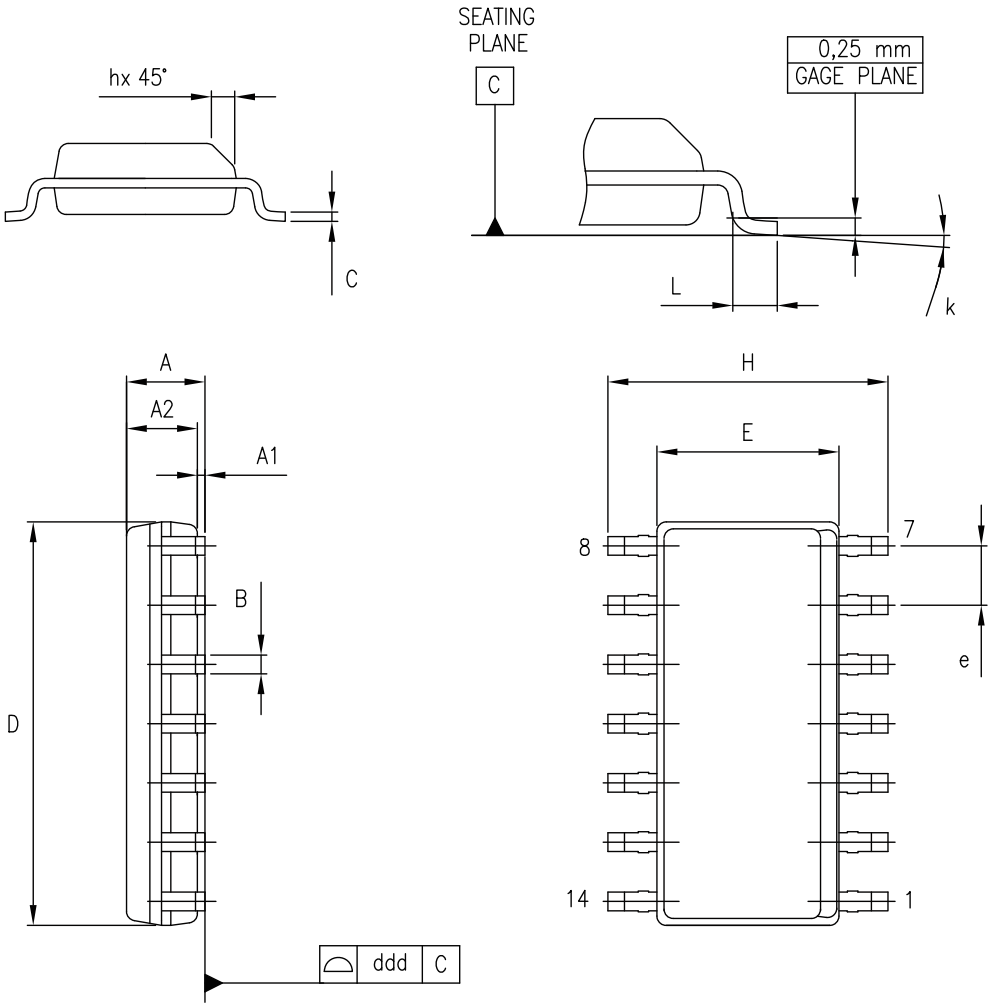
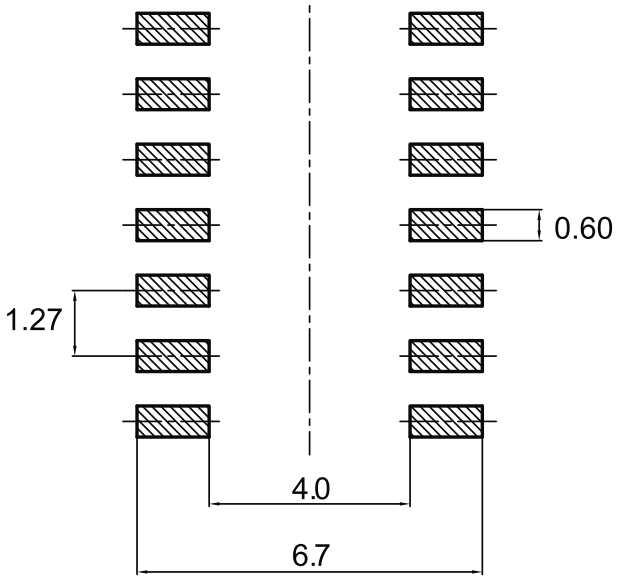


Table 7. **SO-14 package mechanical data**

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	1.35	-	1.75
A1	0.10	-	0.25
A2	1.10	-	1.65
B	0.33	-	0.51
C	0.19	-	0.25
D	8.55	-	8.75
E	3.80	-	4.00
e	-	1.27	-
H	5.80	-	6.20
h	0.25	-	0.50
L	0.40	-	1.27
k	0	-	8
ddd	-	-	0.10

Figure 10. **SO-14 package suggested land pattern**



9 Ordering information

Table 8. **Order code**

Order Code	Package	Package marking	Packing
L6494LD	SO-14	L6494LD	Tube
L6494LDTR	SO-14	L6494LD	Tape and reel

Revision history

Table 9. **Document revision history**

Date	Version	Changes
08-Feb-2017	1	Initial release.
14-Nov-2017	2	Updated Section Description, Table 4 and Table 5
01-Aug-2024	3	Updated Table 5 (DT values and I_{qccu}, I_{qcc}, I_{so}, I_{si} test conditions) and Figure 5 (equation). Updated Table 7 (typo error) and Section 7.

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