PL130-09

High Speed Translator Buffer to LVDS

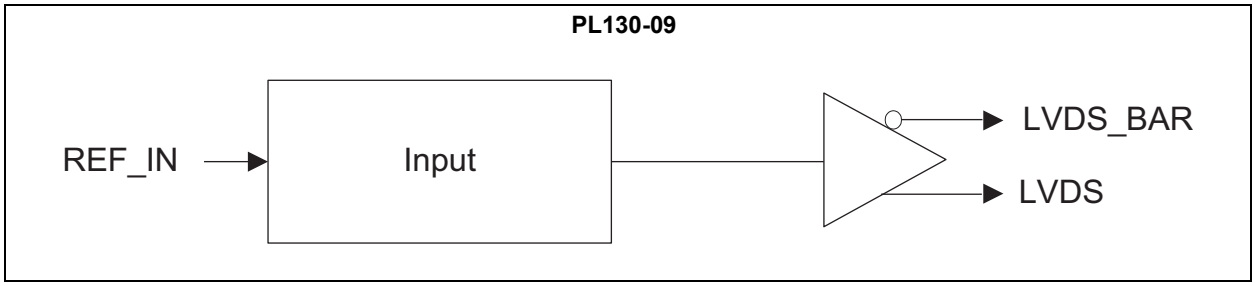
Features

- Differential LVDS Output
- Single AC-Coupled Input (Min. 100 mV Swing)
- Accepts LVCMOS or Sine Wave Inputs
- Input Range from 10 MHz to 1.0 GHz
- 2.5V to 3.3V Operation
- Available in 8-Pin SOIC or 3 mm x 3 mm QFN GREEN/RoHS Compliant Packaging

General Description

The PL130-09 is a low cost, high performance, high speed, buffer that reproduces any input frequency from 10 MHz to 1.0 GHz. It provides a pair of differential LVDS output. Any input signal with at least 100 mV swing can be used as reference signal. This chip is ideal for conversion from sine wave, TTL, CMOS, or PECL to LVDS.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{DD}) .....+4.6V
Input Voltage (DC).....–0.5V to V_{DD} + 0.5V
Output Voltage (DC).....–0.5V to V_{DD} + 0.5V
HBM ESD Rating.....2 kV

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

GENERAL ELECTRICAL CHARACTERISTICS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Current, No Load	I_{DD}	—	25	30	mA	F_{OUT} = 200 MHz, LVDS
Operating Voltage	V_{DD}	2.25		3.63	V	—
Output Clock Duty Cycle	—	±5% of input			%	@ 1.25V (LVDS)

AC ELECTRICAL CHARACTERISTICS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Frequency	—	10	—	1000	MHz	—
Input Signal Swing	—	100	—	—	mV	REF_IN input
Output Frequency	—	10	—	1000	MHz	—

LVDS ELECTRICAL CHARACTERISTICS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Differential Voltage	V_{OD}	247	355	454	mV	R_L = 100Ω See Figure 3-1
VDD Magnitude Change	ΔV_{OD}	–50	—	50	mV	
Output High Voltage	V_{OH}	—	1.4	1.6	V	
Output Low Voltage	V_{OL}	0.9	1.1	—	V	
Offset Voltage	V_{OS}	1.125	1.2	1.375	V	
Offset Magnitude Change	ΔV_{OS}	0	3	25	mV	
Power-Off Leakage	I_{OXD}	—	±1	±10	µA	V_{OUT} = V_{DD} or GND, V_{DD} = 0V
Output Short Circuit Current	I_{OSD}	—	–5.7	–8	mA	—

LVDS SWITCHING CHARACTERISTICS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Differential Clock Rise Time	t_r	0.2	0.7	1.0	ns	R_L = 100Ω, C_L = 10 pF See Figure 3-2
Differential Clock Fall Time	t_f	0.2	0.7	1.0	ns	

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T_S	–65	—	+150	°C	—
Ambient Operating Temperature	T_A	–40	—	+85	°C	Note 2
Junction Temperature	T_J	—	—	+125	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 10 seconds

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

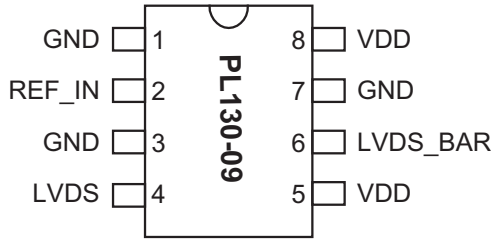
2: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

Pin Configurations

PL130-09
8-Pin SOIC (Top View)



PL130-09
16-Pin QFN (Top View)

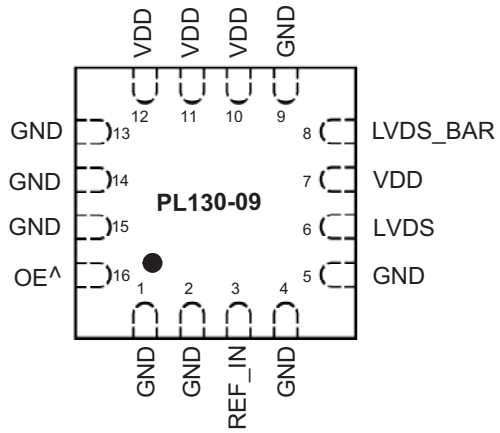


TABLE 2-1: PIN FUNCTION TABLE

Pin Name	SOIC-8L	QFN-16L	Type	Description
GND	1, 3, 7	1, 2, 4, 5, 9, 13, 14, 15	P	Ground.
VDD	5, 8	7, 10, 11, 12	P	Power supply.
REF_IN	2	3	I	Reference input signal. The frequency of this signal will be reproduced at the output (after translation to LVDS level).
LVDS	6	6	O	LVDS true output.
LVDS_BAR	4	8	O	LVDS complementary output.
OE	N/A	16	I	Output enable (‘1’ for enable). Internal pull -up (default is ‘1’).

3.0 TEST CIRCUITS AND WAVEFORM

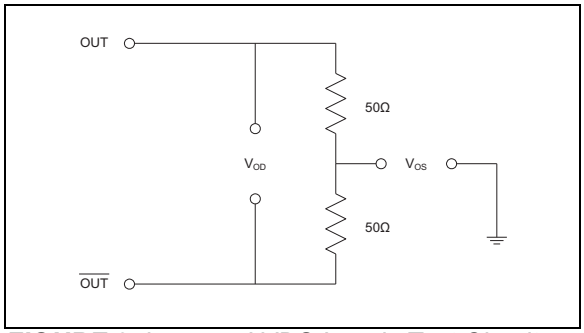


FIGURE 3-1: *LVDS Levels Test Circuit.*

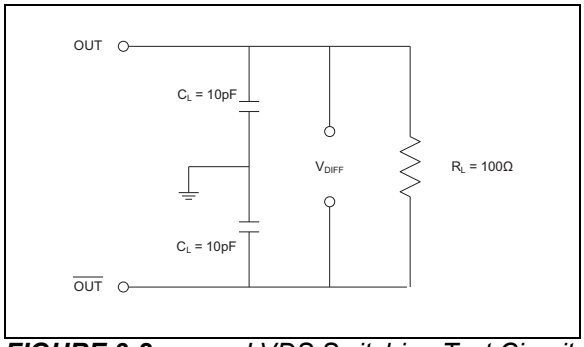


FIGURE 3-2: *LVDS Switching Test Circuit.*

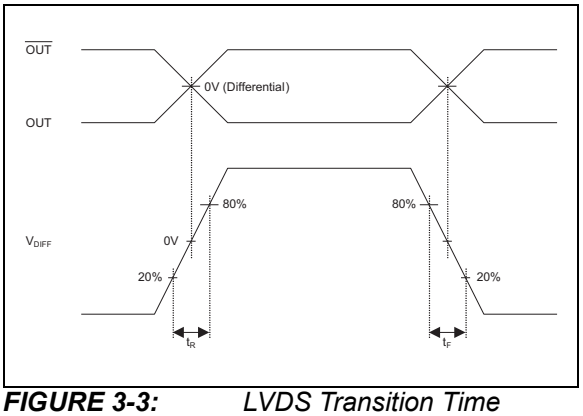
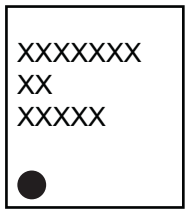


FIGURE 3-3: *LVDS Transition Time Waveform.*

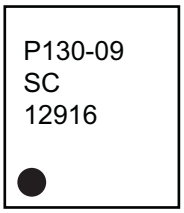
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

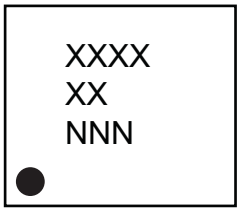
8-Lead SOIC*



Example



16-Lead QFN*



Example

Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

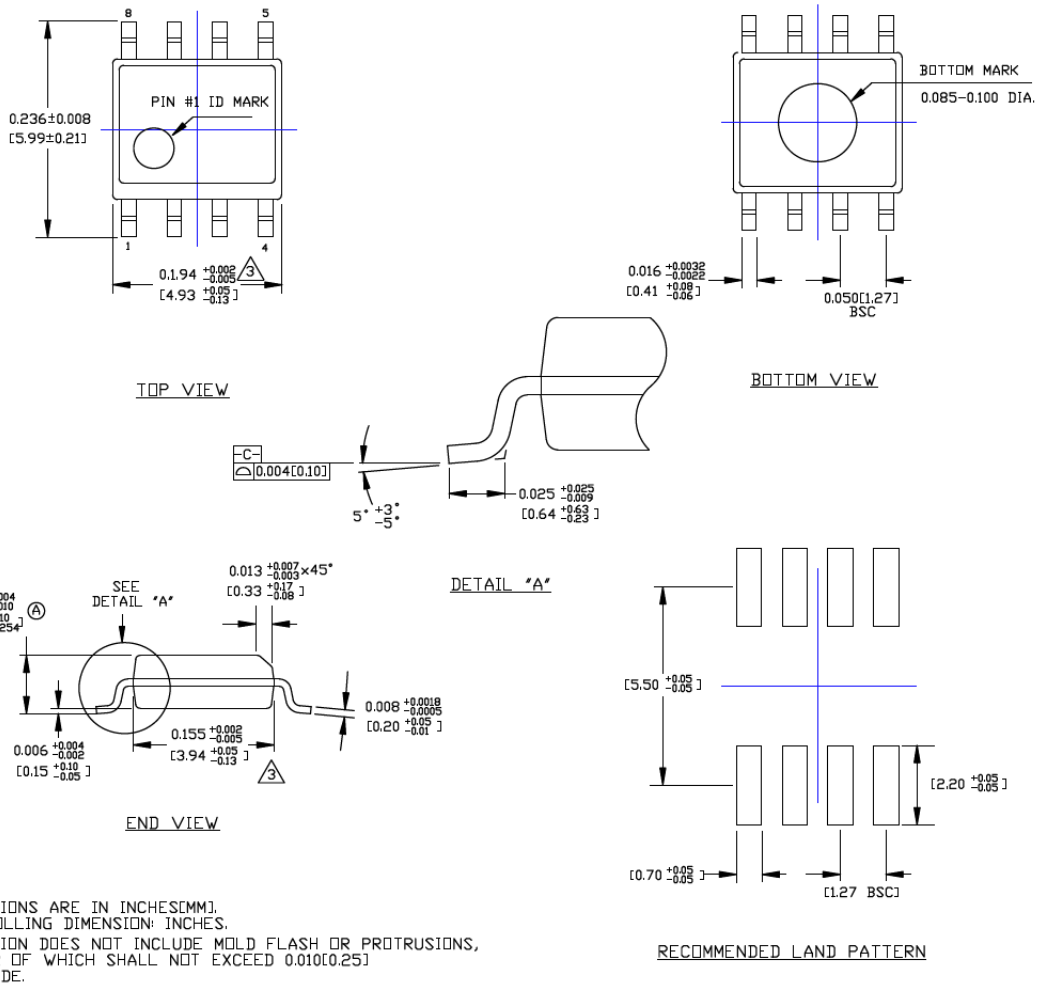
5.0 PACKAGING INFORMATION

8-Lead SOIC Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

TITLE
8 LEAD SOICN PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	SOICN-8LD-PL-1	UNIT	INCH [MM]

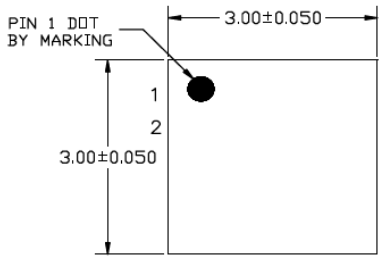


NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.010[0.25] PER SIDE.

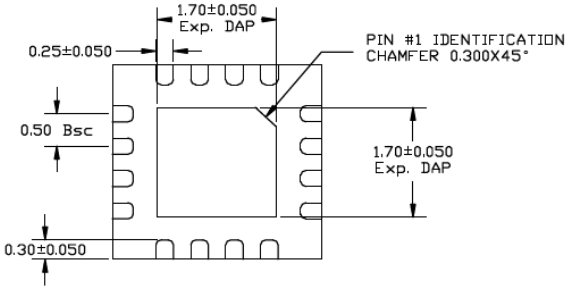
16-Lead QFN 3 mm x 3 mm Package Outline and Recommended Land Pattern

TITLE
16 LEAD QFN 3x3mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

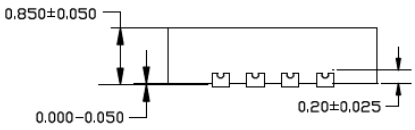
DRAWING #	QFN33-16LD-PL-3	UNIT	MM
Lead Frame	NiPdAu	Lead Finish	NiPdAu



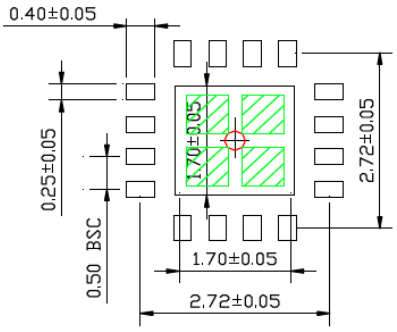
TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3



SIDE VIEW
NOTE: 1, 2, 3



RECOMMENDED LAND PATTERN
NOTE: 4, 5

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED.
4. RED CIRCLE IN LAND PATTERN INDICATES THERMAL VIA. SIZE SHOULD BE 0.30-0.35mm IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE.
5. GREEN RECTANGLES (SHADED AREA) indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.60mm IN SIZE, 0.20mm SPACING.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2020)

- Converted Micrel document PL130-09 to Microchip data sheet DS20006427A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	X
Device	OE State	Package Type	Temperature	Media Type

Device:	PL130-09:	High Speed Translator Buffer to LVDS
OE State:	(blank) =	High Enable
Package Type:	S =	SOIC-8L
	Q =	QFN-16L
Temperature	C =	Commercial Temperature Range
	I =	Industrial Temperature Range
Media Type	(blank) =	100/Tube
	(blank) =	20/Bag

Examples:

a) PL130-09SC: High Speed Translator Inverting Buffer to LVDS, High Enable, SOIC-8L, Commercial Temp. Range, 100/Tube

b) PL130-09QC: High Speed Translator Inverting Buffer to LVDS, High Enable, QFN-16L, Commercial Temp. Range, 20/Bag

c) PL130-09SI: High Speed Translator Inverting Buffer to LVDS, High Enable, SOIC-8L, Industrial Temp. Range, 100/Tube

d) PL130-09QI: High Speed Translator Buffer to LVDS, High Enable, QFN-16L, Industrial Temp. Range, 20/Bag

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
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